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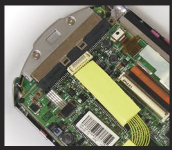

HANDS-ON PROJECT

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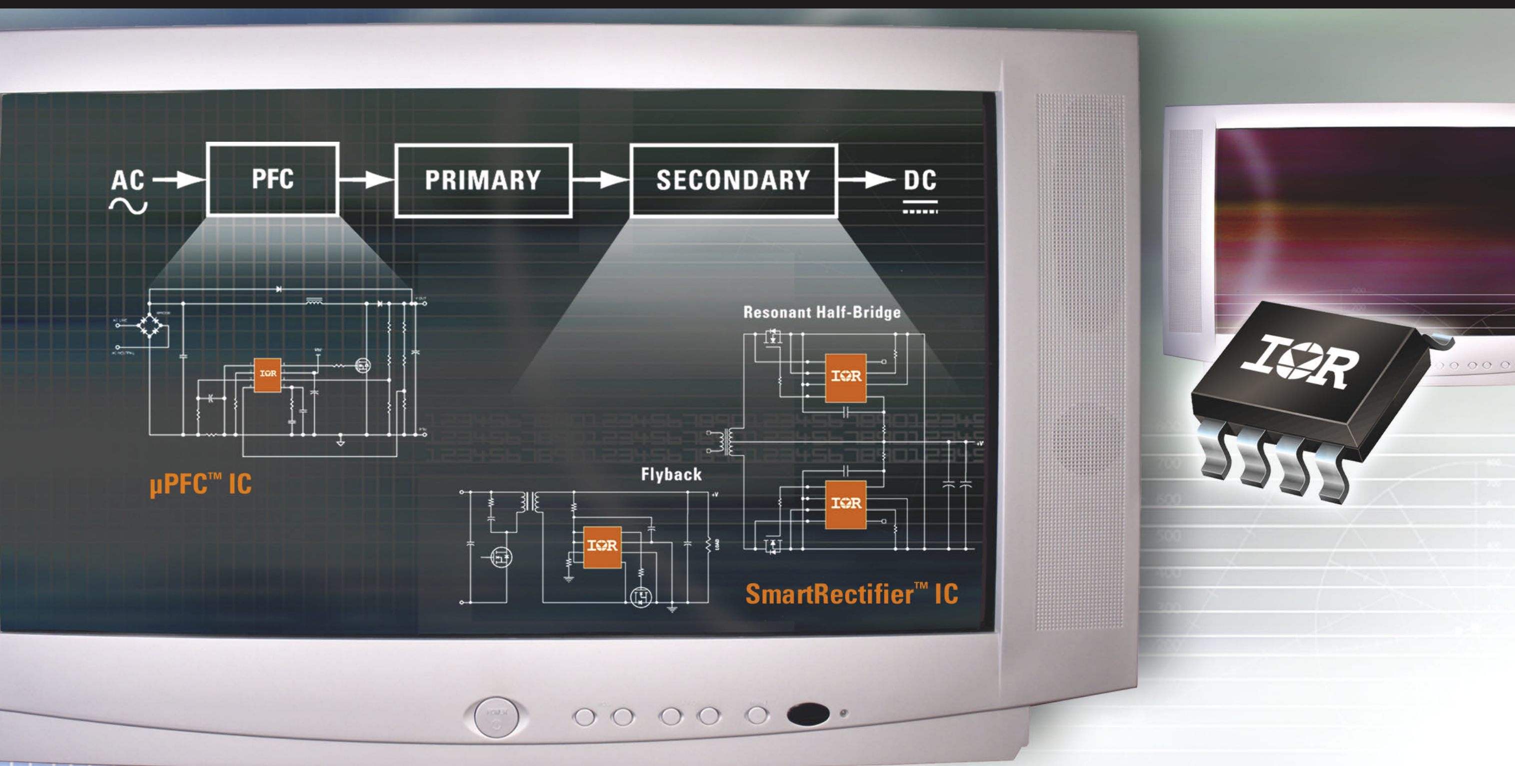

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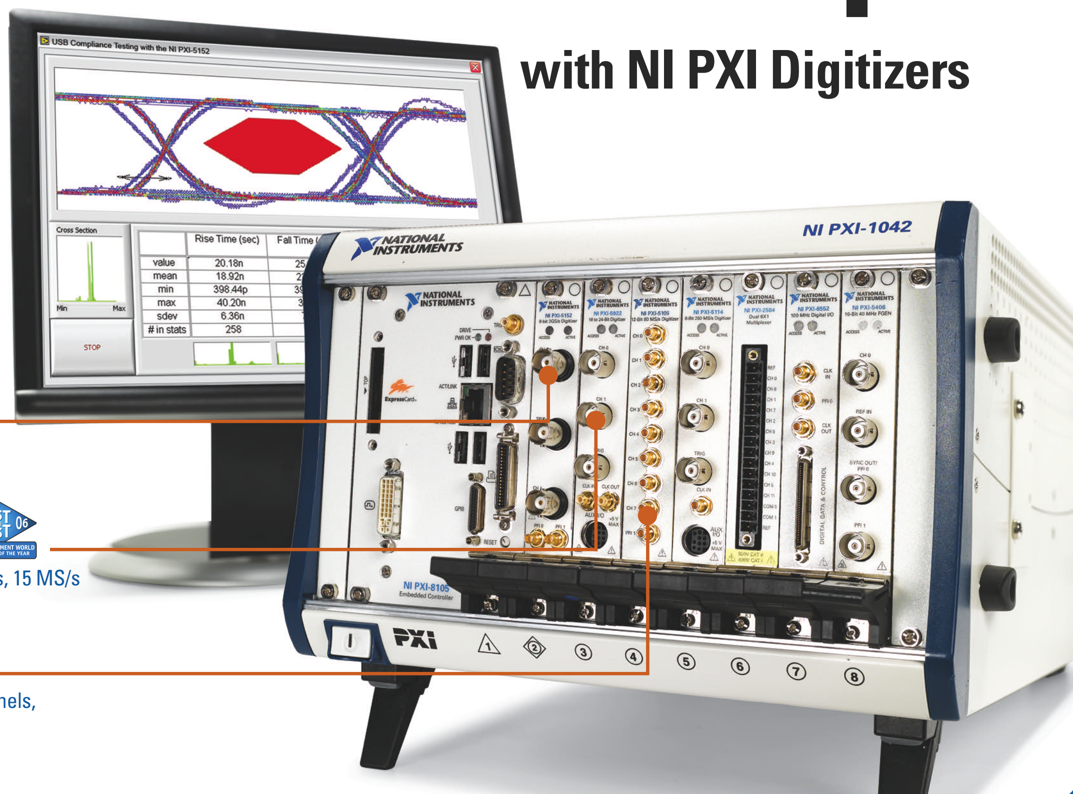

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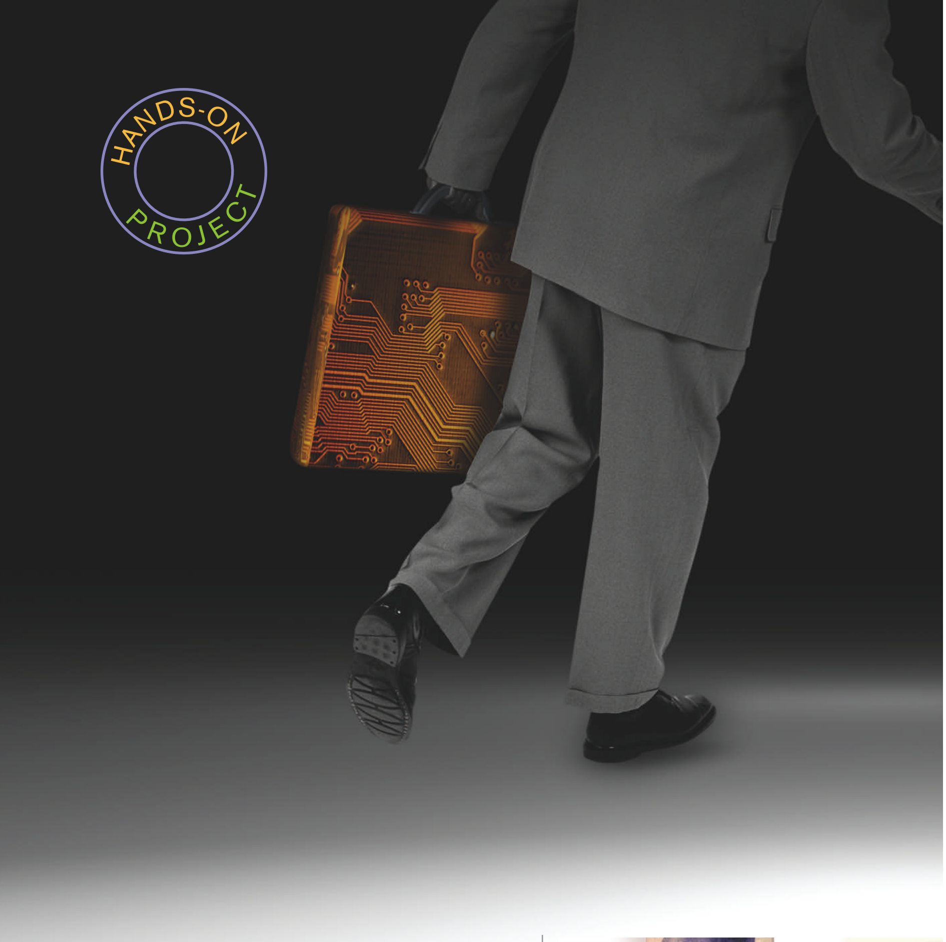

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50 years

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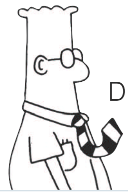

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DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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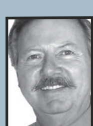

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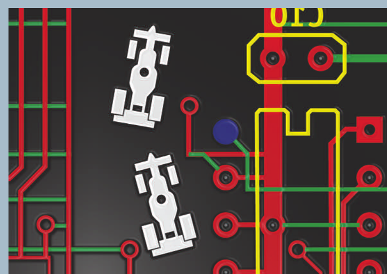

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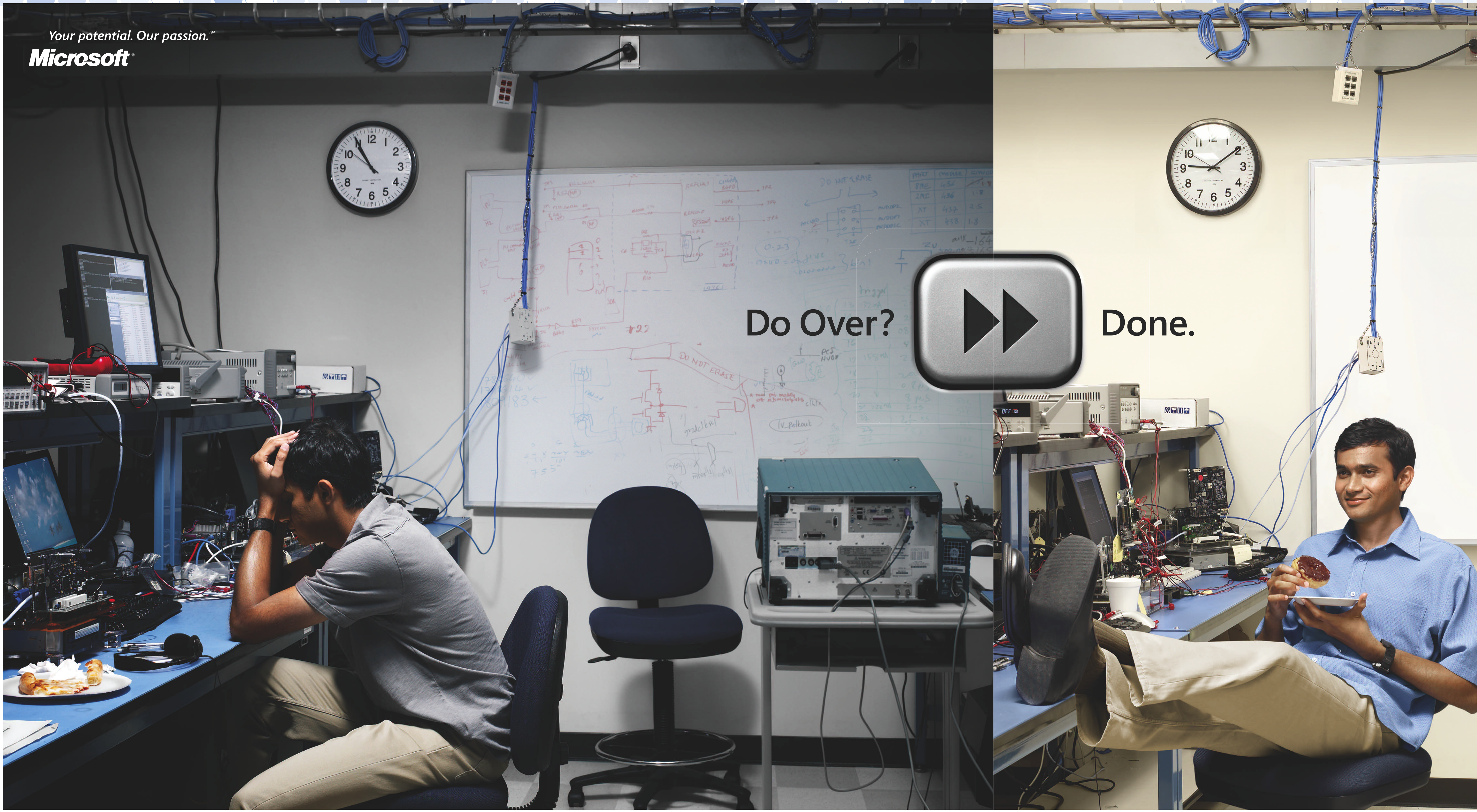

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BY MAURY WRIGHT, EDITOR IN CHIEF

Triple-play update: Telcos falter; cable companies soar

I recently railed against marketers trying to ride the popularity of the term "triple play" in the column "Triple-play trickery: Beware the buzzword bandwagon" (*EDN*, Oct 12, 2006, pg 12, www.edn.com/article/CA6378086). "Triple play" refers to telecom carriers or cable companies offering a bundle of video, Internet, and phone services.

Thinking about that column and prompted by a flurry of news stories and quarterly-results reports, I decided to revisit the topic and look at who is succeeding and failing. In North America, the current landscape is bleak for the telecom side. On the other hand, North America is the only global region with a broad cable deployment. If you are a designer who needs to pick a winner to make decisions on an upcoming product, you face a tough decision.

As I write this, Verizon has just announced quarterly results. The company did great in the mobile-phone-service sector. In fact, results were generally good, but analysts hammered the company on the performance of its FiOS (fiber-optic services) triple-play offering. Although Verizon is out in front among the telecom carriers in deploying a fiber-optic-based network that can deliver video, the deployment isn't matching analysts' expectations. The company isn't adding subscribers as fast as the analysts would like, customer-acquisition (marketing) costs are higher than expected, and the installation costs of the fiber plant are running high.

There are also technical issues with the FiOS deployment. Microsoft's software has been problematic. Hardware and software deliveries have been late. And the current FiOS deployment is only an interim step. The current technology uses a video-overlay network—essentially a cablelike multicast architecture—whereas Verizon and other carriers ultimately plan to move to IPTV (Internet Protocol TV), in which a converged network carries data, voice, and video packets. (See "100-Mbps broadband: how, why, when, and where?" *EDN*, July 7, 2006, pg 48, www.edn.com/article/CA6347250 for background information.)

But I give Verizon credit for aggressively moving forward. AT&T, in contrast, is struggling mightily with its U-verse trial in Texas. About the time the Verizon results hit, *USA Today* ran an article called "AT&T cable plan includes wireless" (www.usatoday.com/money/industries/telecom/2006-10-31-att-usat_x.htm), which revealed that AT&T has yet to offer HDTV (high-definition-TV)-resolution content through U-verse and that only 3000 subscribers have signed on. Now, AT&T is doing trials on true IPTV technology. And the company claims that it will be in 15 to 20 markets by the end of the year. But, with the calendar turned to November, I'm almost positive that scenario won't happen. I can only guess that the AT&T article was the result of spin-doctoring. Read the story, and you'll learn that mobile service is somehow going to be AT&T's secret weapon in winning video customers.

Meanwhile, Time Warner (www.timewarner.com) also just announced results that the business press described as "soaring." The press largely attributes this achievement to the company's success in going against the telecom carriers. And I just don't buy that the lack of a wireless-phone-services offering—a "quad play"—is going to derail the cable guys.

So, where do you place your bets? The uncertainty affects small companies to behemoths. In my blog post "Texas Instruments and Ikanos rev DSL chip offerings: Is anyone buying?" (www.edn.com/blog/150000015.html), I covered some exciting new VDSL2 ICs that could enable video delivery over copper phone lines. But neither company can point to significant deployment of VDSL2 chips. And deploying those chips in a sense future-proofs a network because the chips can support ADSL2/2+ services today and faster VDSL2 services tomorrow. Texas Instruments has yet to even announce a PON (passive-optical-network) chip, although I surely expect them to, given the company's success in other broadband technologies. I can only guess that TI is waiting for the technology to mature and that company officials don't feel like it is losing enough business to matter in early deployments. In fact, TI just entered the VDSL2 market.

The bad news here centers on the fact that converged networks should now be huge drivers of the tech industry. Designers working on everything from home-networking products to new software products would benefit. Here's hoping that the next quarter is brighter across the board. Triple play will be a global-tech driver, and the cable guys can't help in much of the world. **EDN**

Contact me at mgwright@edn.com.

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SY89856U	1:6 Fanout w/ 2:1 Input MUX	Yes	5mm x 5mm	$3.79
SY89858U	1:8 Fanout	Yes	5mm x 5mm	$3.79
SY89112U	1:12 Fanout w/ 2:1 Input MUX	Yes	7mm x 7mm	$4.24
		Multiplexers (MUX)		
SY89852U	2:1 MUX	Yes	3mm x 3mm	$2.15
SY89853U	Dual 2:1 MUX	Yes	5mm x 5mm	$3.25
SY89855U	4:1 MUX	Yes	5mm x 5mm	$3.35
SY89859U	8:1 MUX w/ 1:2 Fanout	Yes	5mm x 5mm	$5.95

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EDITED BY FRAN GRANVILLE

pulse

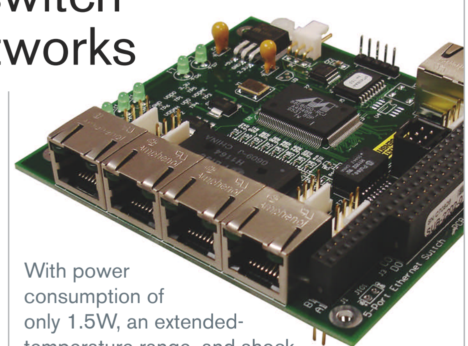
INNOVATIONS & INNOVATORS

PC/104 Ethernet switch supports virtual networks

With high-reliability aviation, industrial, military, and transportation applications in mind, Parvus recently introduced the five-port PRV-1059 Fast Ethernet switch. The module features low power consumption, high shock resistance, and extended-temperature operation to 85°C in a PC/104 form factor. The switch enables you to network together as many as five embedded-computing devices using 10BaseT or 100BaseTX connections. The PRV-1059 also supports field-programmable, port-based VLAN functions enabling you to connect any combination of ports in subnets for use in small, independent networks.

You can use the module either as a standalone network switch with no processor board or in combination with embedded systems that support a PC/104 ISA bus. The PRV-1059 switch has a list price of $199 for base models and $249 for models with VLAN support.**—by Warren Webb**

▷**Parvus Corp**, www.parvus.com.



With power consumption of only 1.5W, an extended-temperature range, and shock resistance, the PC/104-based PRV-1059 Ethernet switch features field-programmable virtual networking.

FROM THE VAULT

"AT&T Microelectronics announced ... its BEST-I (bipolar enhanced self-aligned technology) process. The process allows for the fabrication of gates with speed/power combinations (of) 80 psec at 2 mW/gate to 200 psec at 0.75 mW/gate. The transistors' toggle frequency is 3 GHz."

—*EDN*, May 25, 1989, pg 19

Input board shrinks data-acquisition footprint

United Electronic Industries' new DNA-AI-225 analog-input board features 25 differential-input channels, each with 24-bit resolution and a maximum sampling rate of 1k sample/sec. With a separate ADC for each input, the unit can simultaneously sample all 25 channels, thus eliminating the noise and offset errors associated with multiplexed inputs. The board fits the vendor's PowerDNA (Distributed Networked Automation) Cube, a 4×4×5.8-in., Ethernet-based data-acquisition system targeting industrial, aerospace, in-vehicle, and laboratory applications.

Using the DNA-AI-225, you can fit as many as 150 analog-input channels into a single chassis. The board includes software drivers for Windows, LabView, Matlab, Linux, and most real-time operating systems. The DNA-AI-225 sells for $1600 and is available now.**—by Warren Webb**

▷**United Electronic Industries**, www.ueidaq.com.

The DNA-AI-225 analog board provides 25 differential-input channels for the PowerDNA data-acquisition system.

Virtex-5 adds PCI Express, 10-Gbit-Ethernet cores

Xilinx has released the second platform derivative of its Virtex-5 FGPA family targeting markets requiring serial connectivity. Xilinx this year also unveiled its top-of-the-line Virtex-5 FPGAs, the first FPGAs in the industry at the 65-nm node. The new devices feature a six-input-look-up-table architecture and some design and foundry tricks to keep power consumption on par with the company's 90-nm Virtex-4 FPGAs and still gain the usual performance and price-per-gate advantages of process reductions. When Xilinx announced the family, the company also released the LX base platform, which is a pure-logic, sea-of-gates FPGA. Now, the company is releasing derivative platforms of the Virtex-5 targeting specific markets.

The first of these derivative platforms, the Virtex-5 LTX, includes a lot of logic, as does the LX, but adds several hard blocks of serial I/O to help designers targeting the "triple play"—video, data, and voice—for markets requiring serial connectivity. Balaji Thirumalai, senior manager of Virtex marketing at Xilinx, says that designers in the wired- and wireless-communications market have been the traditional targets for these types of devices, but triple-play serial connectivity is now starting to displace parallel connectivity and is making its way into other applications, such as consumer electronics, audio/video broadcast, automotive, aeronautics and defense, storage, and servers.

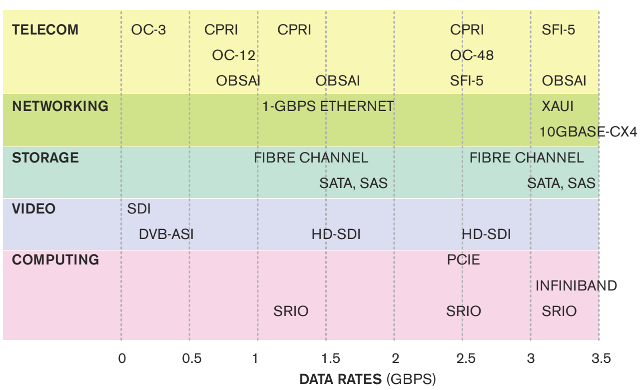
"We introduced serial I/O in Virtex-II Pro and Virtex-4, and, over the years, customers became comfortable with having FPGAs with SERDES [serializer/deserializer] features," says Thirumalai. "Those customers were typically in the communications and networking areas and willing to take risks with leading-edge technology. They wanted the highest performance and data rates. Now, as the mainstream market starts to adopt serial rather than parallel I/O, the market has slightly different needs." The biggest difference, says Thirumalai, is that most of the mainstream applications don't call for blazingly fast I/O and are typically operating at speeds of less than 3.2 Gbps.

Xilinx claims that LTX helps designers target applications in this sweet spot. Thus, it integrates PCIe (PCI Express) and Ethernet MAC (media-access-controller) hard cores into the fabric. The hard cores include RocketIO transceivers, which give the LTX speed as great as 3.2 Gbps with typical power consumption of 100 mW. The LTX Ethernet support includes four independent 10/100/1000-Mbps blocks that work with RocketIO transceivers, and the PCIe support includes a PCIe endpoint block that works with the RocketIO transceivers to give users access to one-, two-, four-, and eight-lane PCIe interfaces. With those blocks, the LTX can support PCIe, Gigabit Ethernet, XAUI (extended attachment-unit-interface), and OC-48 protocols, among others.

The company initially released the 5VLX30T, 5VLX50T, and 5VLX110T LTX versions, which have 30,000, 50,000, and 110,000 look-up tables, respectively. The company is offering sample silicon of these devices and plans full production for early 2008. The company also plans to offer an 85,000-look-up-table LX85T and 330,000-look-up-table LX330T. In 2008, the LX30T, LX50T, and LX110T devices will sell for $109, $189, and $529 (1000), respectively. The next platform on the company's Virtex-5 road map adds a DSP as well as serial I/O to FPGA logic. Xilinx plans to announce that device during the first half of next year.

—by Michael Santarini

▷**Xilinx**, www.xilinx.com.



NOTES: CPRI: COMMON PUBLIC-RADIO INTERFACE.
SFI: SERDES FRAMER INTERFACE.
OBSAI: OPEN-BASE-STATION-ARCHITECTURE INITIATIVE.
XAUI: EXTENDED ATTACHMENT-UNIT INTERFACE.
ASI: ASYCHRONOUS SERIAL INTERFACE.
SRIO: SERIAL RAPIDIO.
SDI: SERIAL DIGITAL INTERFACE.

The Virtex-5 LTX includes a lot of logic, as does the LX, but adds several hard blocks of serial I/O to help designers targeting the "triple play"—video, data, and voice—for markets requiring serial connectivity.

DILBERT By Scott Adams

Upgrade Your DAC Designs

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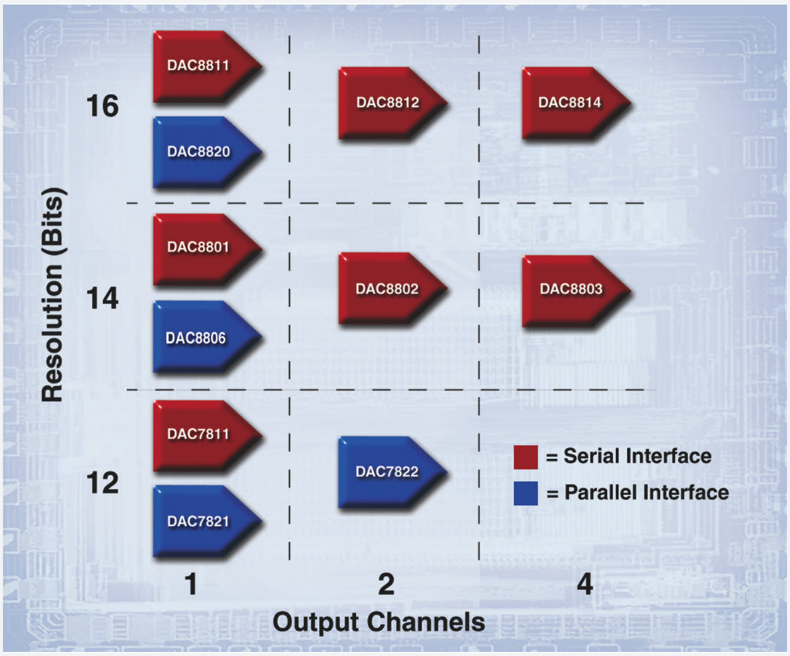

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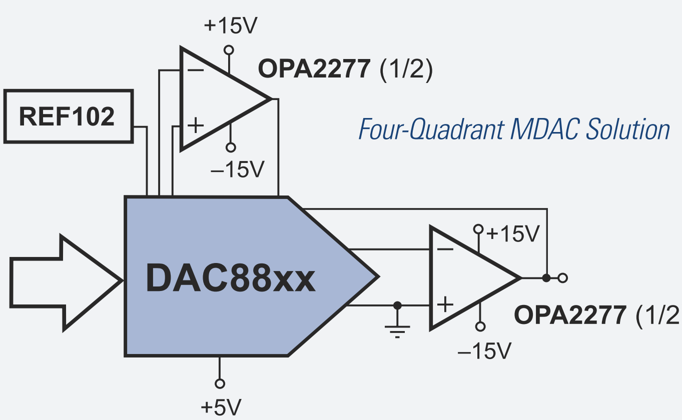

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Two suppliers' handheld DMMs offer differing features

Vendors have crowded the handheld-DMM (digital-multimeter) market for almost as long as it has existed. To many in the industry, Fluke is synonymous with handheld DMMs. Industry watchers, however, have never regarded T&M-product-leader Agilent Technologies as a key player in handheld DMMs, even though its annual revenues are several times Fluke's. In the DMM arena, Agilent is best known for its benchtop units. Now, though, only about a month apart, both Agilent and Fluke have introduced handheld-DMM lines. The Agilent units offer higher resolution at prices higher than those of Fluke's units. Time will tell whether the new entry noticeably affects Fluke's DMM revenues or whether Agilent will prove to be just another of the many competitors that Fluke has learned are facts of life.

Fluke has taken an unusual approach to the array of capabilities it offers in each of its four new true-rms-reading (for ac measurements) ±6000-count full-scale DMMs: the $129.95 114 for electrical troubleshooting, the $149.95 115 for field service, the $169.95 116 for HVAC (heating, ventilating, and air conditioning), and the $179.95 117 for electricians. Instead of the "good-better-best" approach the DMM industry has long used, the new units offer capabilities tuned to the needs of different user groups. Aside from the meters' basic functions, several of those capabilities depart significantly from those of Agilent's new units.

The true-rms-reading Agilent U1252A (left) features a dual display and a full-scale range of ±50,000 counts. Neither feature is common in handheld DMMs. The Fluke 117 (right) is a member of a new DMM family that departs from the industry's time-honored "good-better-best" approach to determining features and, instead, focuses on the requirements of different groups of users.

All four Fluke models are Category III 600V safety-rated and feature large, white-LED-backlit displays and compact design for one-handed operation. The 116 and 117 are also available as parts of easy-to-carry kits that provide additional instruments and accessories. In addition, the 117 includes VoltAlert noncontact voltage detection, which quickly senses the presence of ac voltage; Auto-V automatic voltage detection, which automatically determines a voltage's range and whether it is ac or dc; and a new low-impedance input function, which helps prevent false readings resulting from "ghost" voltages.

Agilent claims that its U1250A-series of true-rms-reading handheld DMMs, whose US prices start at $399, emphasize the company's commitment to offering affordable solutions to test-and-measurement problems. Electronics engineers and technicians increasingly need high-performance portable instruments for service and maintenance. Agilent says that its new products address these needs, enabling users to perform tests in the plant and offsite without compromising measurement integrity.

Benefits of the U1251A and U1252A include precise measurements. The models provide 4½-digit resolution with ±50,000 counts full-scale on a dual display and basic error limits as low as 0.025%, enabling simultaneous, accurate measurements and allowing either quick validation or tolerance checks and marginal-failure troubleshooting. The models also provide versatility: Besides the basic measurement functions, the devices offer automated data logging through an optional PC-interface cable, a 20-MHz frequency counter, a programmable square-wave generator, and temperature measurement. The devices also tout durability and safety: Both of the Category III 1000V-rated models come in a robust package with a shock-absorbing overmold. Rated specifications apply from −20 to +55°C.

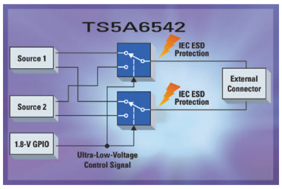
—by Dan Strassberg

▷**Agilent Technologies**, www.agilent.com/find/U1250A_pr.

▷**Fluke Corp**, www.fluke.com.

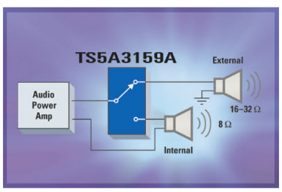
FROM THE VAULT

"The state of the art in Winchester drives changes constantly, and, in 1989, you have higher capacity drives ... in every form factor. Several companies ship 5¼-in., full-height, 760-Mbyte products, and two have introduced 1.2-Gbyte drives. Half-height, 5¼-in. offerings include 380-Mbyte drives, and the capacities of 3½-in. drives exceed 200 Mbytes."—*EDN*, May 25, 1989, pg 122



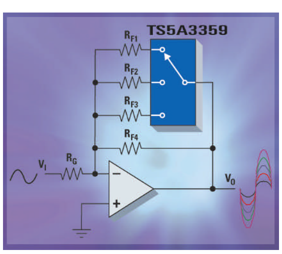
▶ Single SPDT analog switch with input logic translation and IEC ESD (TS5A6542)

- +/- 15kV IEC 61000-4-2 Contact Discharge ESD protection (common pin)
- Low ON-state resistance (0.75Ω max)
- Excellent ON-state resistance matching
- Break-before-make switching



▶ Single 0.9-Ω SPDT analog switch (TS5A3159A)

- 100-MHz bandwidth – highest of any 3159-type in the industry
- Ultra-small wafer chip scale packaging
- Wide low-voltage operating range: 1.65 V to 5.5 V
- Break-before-make switching



▶ Single, 0.9-Ω SP3T analog switch (TS5A3359)

- Space-saving integration eliminates the need for using serial connected SPDT analog switches
- Isolation in the powered down mode (V+ = 0V)
- 1.65-V to 5.5-V single-supply operation (Control Inputs are 5.5 V tolerant)
- Break-before-make switching

Analog Switches from Texas Instruments

Device	r_{on}* (Ω) (max)	r_{on} Flatness (Ω) (max)	r_{on} Mismatch (Ω) (max)	V_+ (V) (min)	V_+ (V) (max)	ON Time (ns) (max)	OFF Time (ns) (max)	Pins/Packages
SPST								
TS5A3166	0.9	0.15	—	1.65	5.5	7	11.5	5/SC70, SOT-23, WCSP
TS5A3167	0.9	0.15	—	1.65	5.5	7	11.5	5/SC70, SOT-23, WCSP
TS5A4594	8	1.5	—	2.7	5.51	7	14	5/SC70, SOT-23
TS5A4595	8	1.5	—	2.7	5.51	7	14	5/SC70, SOT-23
TS5A4596	8	1.5	—	2.7	5.5	17	14	5/SC70, SOT-23
TS5A4597	8	1.5	—	2.7	5.5	17	14	5/SC70, SOT-23
TS5A1066	10	5	—	1.65	5.5	5.5	4.5	5/SC70, SOT-23, WCSP
SPST x 2								
TS5A23166	0.9	0.25	0.1	1.65	5.5	7.5	11	8/US8, WCSP
TS5A23167	0.9	0.25	0.1	1.65	5.5	7.5	11	8/US8, WCSP
TS3A4741	0.9	0.4	0.05	1.65	3.6	14	9	8/SSOP, MSOP
TS5A2066	10	5	1	1.65	5.5	5.8	3.6	8/SM8, US8, WCSP
SPST x 4								
TS3A4751	0.9	0.4	0.05	1.65	3.6	14	9	14/TSSOP
SPDT								
TS5A6542	0.75	0.25	0.25	2.25	5.5	25	20	8/WCSP
TS5A4624	0.9	0.25	0.1	1.65	5.5	22	8	6/SC70
TS5A3153	0.9	0.15	0.1	1.65	5.5	16	15	8/US8, WCSP
TS5A3154	0.9	0.15	0.1	1.65	5.5	8	12.5	8/US8, WCSP
TS5A3159A	0.9	0.25	0.1	1.65	5.5	30	20	6/SC70, SOT-23, WCSP
TS5A3159	1.1	0.15	0.1	1.65	5.5	35	20	6/SC70, SOT-23
TS5A3160	0.9	0.25	0.1	1.65	5.5	6	13	6/SC70, SOT-23
TS5A3157	10	5	0.2	1.65	5.5	8.5	6.5	6/SC70, SOT-23, WCSP
TS5A63157	10	2	0.14	1.65	5.5	5	3.4	6/SC70, SOT-23
TS5A2053	13.8	4.5	4.5	1.65	5.5	6.8	4.1	8/SM8, US8
SPDT x 2								
TS5A23159	0.9	0.25	0.1	1.65	5.5	13	8	10/MSOP, QFN
TS5A23160	0.9	0.25	0.1	1.65	5.5	5.5	10	10/MSOP
TS5A23157	10	4(typ)	0.15(typ)	1.65	5.5	5.7	3.8	10/MSOP
SPDT x 4								
TS3A5018	10	7	0.8	1.65	3.6	8	6.5	16/SOIC, SSOP (QSOP), TSSOP, TVSOP,QFN
SP3T								
TS5A3359	0.9	0.25	0.1	1.65	5.5	21	10.5	8/US8
TS5A3357	15	6.5(typ)	0.1(typ)	1.65	5.5	6.5	3.7	8/SM8, US8
SP4T x 2								
TS3A5017	12	9	2	2.3	3.6	9.5	3.5	16/SOIC, SSOP (QSOP), TSSOP, TVSOP, QFN

**Data measured under typical conditions with maximum V_+.*
Data collected as of 7/06

*New Products are listed in **bold red.***

5-ball/6-ball WCSP (YZP)
Ball pitch = 0.020 mm (0.50 mm)
Height = 0.020 mm (0.50 mm)
Area = 0.002 mm (1.26 mm)

10-pin QFN (RSE)
Lead pitch = 0.020 mm (0.50 mm)
Height = 0.039 mm (0.60 mm)
Area = 0.005 mm (3.18 mm)

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VOICES

Amir Majidimehr: a "window" to the world of telecom

EDN interviewed Amir Majidimehr, corporate vice president of the Consumer Media Technology Group within the Mobile and Embedded Devices Division at Microsoft. His team delivers Microsoft digital-media technology to mobile operators and consumer-electronics manufacturers and owns Microsoft's digital-rights-management and advanced-media strategies, including HD DVD. This is an excerpt of that interview. You can find the complete interview online at www.edn.com/061123p1.

Microsoft in late 2001 unveiled its Corona audio and video codecs, which it later renamed the Windows Media 9 series. They delivered significant feature and quality advancements over their predecessors, but, five years later, Version 9 is still the latest and greatest Windows Media variant. When should we expect to see the next major Windows Media upgrade, what will it accomplish, and will it be bit-stream-compatible with earlier audio and video decoders?

A In the early days of Windows Media development, Microsoft mainly focused on Web streaming on PCs. We had the luxury of power and convenience of the Internet to greatly ease the decoder download to PCs. Thus, we didn't have to be concerned about the decoder compatibility too much and thus could come up with new codec formats every year. But we soon realized that the great strength, quality, and flexibility of Windows Media should not be limited to PCs.

Because of this situation, when we designed the WMV9 (Windows Media Video 9) bit-stream syntax and decoding process, we spent extra time making sure that the bit-stream design was flexible and extensible before we shipped it as part of the WMV9 Series so that we can continue to make encoding improvements. We also came up with the Advanced Profile of WMV9 to improve the interlaced mode and made the bit stream even more flexible so that the codec elementary stream could be mapped to any file container, such as MPEG-2 Program Stream and Transport Stream. We then submitted the entire spec to SMPTE [Society of Motion Picture and Television Engineers] for standardization, and it became VC-1.

Since then, we have made a lot of quality and speed improvements on the encoder side for various applications. We submitted WMV9/VC-1 to the DVD Forum for consideration as a mandatory codec for the next-generation high-definition DVD format. We won both DVD Forum tests conducted in late 2002 and early 2003. This win led to VC-1's being chosen as one of the three mandatory codecs for both HD DVD and BD [Blu-ray Disc]. From that point on, we have also worked with studios and post [production] houses to continue improving the VC-1 encoder for HD encoding. We have also developed very powerful VC-1 encoding and analysis tools for HD production. This VC-1 encoder and tool set have become the tools that HD DVD and BD post houses are using today for HD production. Consumers are greatly enjoying the excellent picture quality of HD. It is all a result of the work we put into this.

The market standoff between Blu-ray and HD DVD shows no signs of ending any time soon. Do you agree with this pessimistic view of current events?

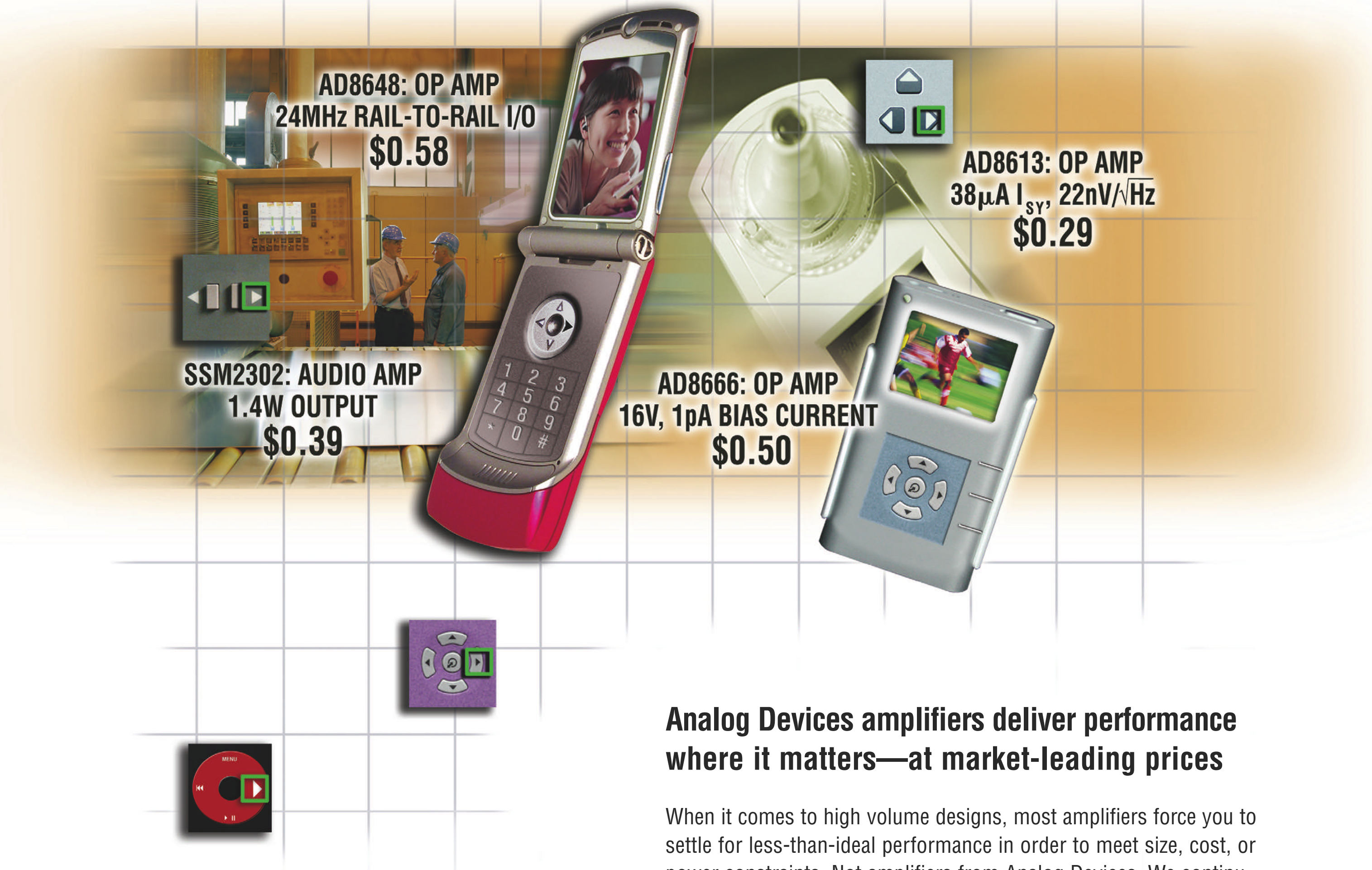
A We're happy with how HD DVD is doing so far. From reviews to blogs to the AVS [Audio Video Science] Forum [www.avsforum.com], we're seeing on par a much better response to HD DVD. The players are better, there's a larger selection of titles, and there's a much higher consistent quality of the titles. I'm also seeing positive response to our decision to offer HD DVD playback as an accessory for the Xbox 360 instead of making every customer pay for it as part of the core console. We're also seeing consumers buying far more HD DVD players and titles than Blu-ray; the latest Nielsen and Video Scan numbers are showing an amazing rate for HD DVD titles.

At the Audio Engineering Society Convention in early October, two Microsoft engineers presented a visionary argument about why, as fiber-to-the-home and other high-bandwidth broadband connections become more pervasive and as hard-drive storage becomes ever-cheaper, downloadable standard- and high-definition audio and video media will increasingly dominate at the expense of traditional packaged media. Do you agree with this assessment?

A Well, first off, there's definitely still a place for new packaged media. We've been supporting the HD DVD format, for example. With disks at 30 Gbytes and beyond, it can be inconvenient to download. Another factor is that online delivery today usually means more compression, which means lower quality. Those looking for the optimal experience will continue to look toward shiny discs until the pipes are bigger.

I think we'll see electronic delivery of video evolve the way we saw it for audio. … The publishers don't need to make a bet on the title for replication and distribution. They can just make the master, and, if it doesn't sell, they're just out the cost of preparing the assets.**—by Brian Dipert**

Amplifier pricing where you want it, performance where you need it, analog is everywhere.



Analog Devices amplifiers deliver performance where it matters—at market-leading prices

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ANALOG DEVICES

GLOBAL DESIGNER

Interface chip provides complete USB connectivity

FTDI (Future Technology Devices International) has extended its series of USB-interface chips with the introduction of the Vinculum family of embedded USB-host controllers. FTDI has designed the ICs to be usable by designers who have no specialist knowledge of the USB standard; the devices handle the USB-host-interface and data-transfer functions and also incorporate an 8/32-bit microcontroller core with embedded flash memory, which enables them to encapsulate the USB-device classes.

You can use the chips to provide a USB-host capability in products that previously lacked the necessary hardware resources. When interfacing to mass-storage devices, such as USB flash drives, Vinculum uses a command set to transparently handle the file-allocation-table structure, communicating through UART, SPI, or parallel-FIFO interfaces. The embedded firmware is complete, and you need not license any further USB software stacks.

The initial product member of the family is the VNC1L device, which features two USB 2.0 ports that firmware can individually configure as host or slave ports. Onboard features include dual DMA controllers for hardware acceleration, 64 kbytes of embedded flash memory for program storage, a 4-kbyte data SRAM, PS2 legacy keyboard and mouse interfaces, and as many as 28 general-purpose-I/O pins. It uses 25 mA from a 3.3V supply, with a 2-mA standby mode, and comes in a 64-pin LQFP outline. The VNC1L's firmware resides in flash memory, and users can upgrade it in the field. The device costs $5 (10,000). FTDI Chief Executive Officer Fred Dart expects users of the chip to add USB-flash-drive connectivity to a wide range of consumer and industrial products.

—by Graham Prophet, *EDN Europe*

▷**FTDI**, www.ftdichip.com, www.vinculum.com.

FEEDBACK LOOP

"I like the idea of doing an actual application, as it would give the ability to overcome the limitation. But ... why not just avoid the hassle ... and just hit the server-based application directly with your Q's browser?"

—Mike Orndorff on *EDN*'s Feedback Loop at www.edn.com/article/CA6382645.

S-band mission payload to launch on W2A satellite

Satellite operator Eutelsat Communications and telecommunications-technology vendor Alcatel announced that Eutelsat will launch an S-band payload on the W2A satellite. According to Alcatel, this decision marks a major success for its strategy to promote mobile TV in the S band in Europe and confirms its vision of the market. The payload employs Alcatel's Alenia Space Spacebus 4000C4 platform; W2A's satellites also comprise as many as 46 transponders in the Ku band and 10 transponders in the C-band payload. With a lifetime of more than 15 years, W2A has a maximum launch mass of 5.7 tons and delivers 11 kW of payload power.

The S-band payload at 2.2 GHz on W2A will allow the delivery, for the first time, of mobile-multimedia-broadcast services, including mobile TV and digital radio, directly onto user terminals over France, Germany, Italy, Poland, Spain, and the United Kingdom. It will therefore initiate the building of a hybrid infrastructure over Europe, combining satellite and terrestrial networks, providing both universal coverage and indoor penetration for mobile-TV services. W2A's S-band payloads will also enable other communications services, such as security communications or crisis management. The W2A satellite will be in orbit in the beginning of 2009. The companies expect that terrestrial deployment could start by the end of 2007.

—by Vinod Kataria, *EDN Asia*

▷**Eutelsat Communications**, www.eutelsat.com.
▷**Alcatel**, www.alcatel.com.

11.23.06

Bipolar transistors achieve speed record

Researchers at the United Kingdom's University of Southampton have produced bipolar transistors that are twice as fast as current devices. Using a standard silicon-bipolar-fabrication technique with fluorine implantation, the group has demonstrated transistors with a transition frequency (f_T) of 110 GHz, a frequency researchers previously have achieved in silicon only by the use of silicon-germanium structures. The fluorine implants, which add little cost to a standard process, suppress boron diffusion in the base of the transistor, resulting in a narrower base width.

University Professor Peter Ashburn believes that researchers may be able to reduce the boron diffusion by another 50%; his group is currently monitoring how the fluorine behaves and looking at whether there are other materials that will also enable this diffusion.

—by Graham Prophet, *EDN Europe*

▶**University of Southampton, www.ecs.soton.ac.uk.**

BY BONNIE BAKER

The difference between latency and settling time for ADCs

Among ADC users, the terms "latency" and "settling time" are sometimes interchangeable. ADC designers, on the other hand, are very clear on the difference between these terms and how these phenomena will affect your application circuits. It is true that ADC users are aware of the effects of these two ADC characteristics on their circuits, but the common misunderstanding of the difference between latency and settling time can cause frustration when a system designer is in the throes of chasing down a signal-integrity problem.

Regardless of whether the converter has an SAR (successive-approximation-register), pipeline, or delta-sigma topology, an ADC's latency is the amount of time that passes from the converter capturing the analog signal until the digital-output word is ready for retrieval. Latency, or delay, includes the conversion time and digital-output time, exclusive of the sampling time. Contrary to the claims on the first pages of some data sheets, latency cannot equal zero. All ADCs take time to complete a conversion from analog to digital.

SAR ADCs have the shortest latency of the most common ADC topologies. After sampling the input signal, most SAR converters start to transmit the digital-output word in as little as one or two clock periods. With pipeline converters, the latency of the digital-output signal depends on the number of internal stages in the pipeline. The latency of pipeline converters is the length of time necessary for all of the internal stages of pipeline to complete the conversion. Pipeline-converter latency also depends on the converter's resolution and is typically six or seven clock periods. Delta-sigma-converter latency is a bit harder to measure. Delta-sigma converters sample the input signal numerous times while sending the sample results to the internal-digital-filter stage. The latency of a delta-sigma converter starts at the beginning of the first sample period and ends when the digital-output data is available to retrieve. The fact that an ADC meets its latency requirements does not ensure that it meets accuracy specifications.

All ADCs take time to complete a conversion from analog to digital.

ADC settling time is a different matter. Settling time is the time necessary for the converter's output to converge to the final value of a step input. SAR-converter settling time, which you measure in seconds, occurs during the acquisition period. Notice that this definition does not include the settling time of the external input filter or the rest of the system. The settling time of pipeline converters is similar to that of SAR converters. Pipeline converters sample the input signal during the acquisition period. To obtain an accurate conversion, the input signal must adequately settle in the analog domain to the resolution levels of the ADC before acquiring the analog signal for the conversion process. Delta-sigma converters differ from both SAR and pipeline converters. The settling time of the internal digital filter in a delta-sigma ADC can reflect the order of the digital filter. You usually measure the settling time of delta-sigma ADCs in cycles; it is equal to the number of conversions necessary for a step input to converge to its final value.

You might conclude from this discussion that the settling time of SAR and pipeline converters is superior to that of delta-sigma ADCs. However, it is useful to think of the system rather than the isolated converter. In the system, SAR and pipeline converters require an external analog filter. This type of filter requires time to settle before the converter can acquire the signal. In contrast, the filter is primarily internal with delta-sigma converters. EDN

ACKNOWLEDGMENT

Special thanks to Michael Ashton, an applications engineer with Texas Instruments, for his insight on delta-sigma converters.

Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

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Comparison Table*

	Agilent LXI Switch/Measure**	NI PXI Switching***
List Price (100 channels)	**$4,779** Uses 2 of 8 slots	$9,190 Uses 5 of 5 slots
List Price (300 channels)	**$9,565** Uses 5 of 8 slots	$21,969 Uses 12 of 14 slots
List Price (500 channels)	**$13,915** Uses 8 of 8 slots	$32,257 Uses 18 of 18 slots
	Features	
I/O to computer	Industry Standard LAN, USB, GPIB	Proprietary PCIe-MXI
Scanning speed	109 chan/sec	140 chan/sec
Size	3U vertical space in rack	4U vertical space in rack
Front panel	Yes	No
Graphical Web interface	Yes	No

Based on a typical data acquisition application with inputs up to 300V multiplexed to a 6 ½-digit digital multimeter for measurements.

Agilent Open

LXI

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 Prices subject to change without notice.

***Based on 34980A pricing and data sheet from www.agilent.com/find/34980A on Sept 29, 2006.*

****Based on PXI switch pricing and data sheet from National Instruments Web site on Sept 29, 2006.*

Agilent Technologies

PRY FURTHER AT EDN.COM

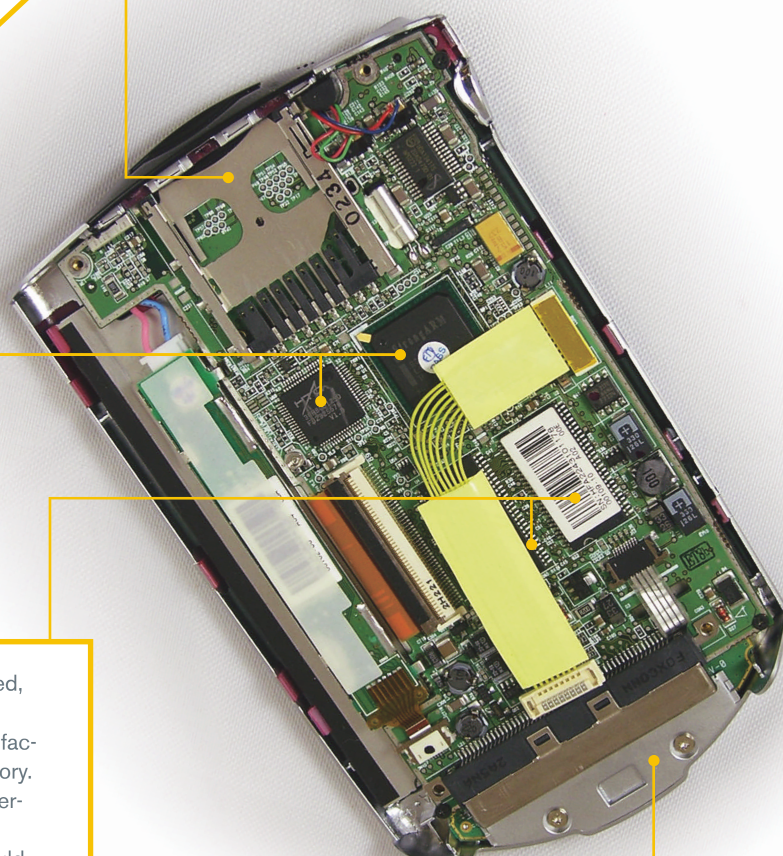
Go to www.edn.com/061123pry for an extended edition of this article.

Piecing together a Pocket PC

A deeply cycled, defunct battery provided a good excuse to crack open a classic: Compaq/HP's popular late-2001 iPaq 3835, whose hardware design formed the foundation of five product-family generations. What did Compaq squeeze inside the 5.29×3.12×0.65-in., 6.4-oz form factor, and what did it omit?

The iPaq 38xx models incorporated a then-state-of-the-art SD (Secure Digital) card socket, which earlier generation iPaq models lacked. Unfortunately, the socket didn't support SDIO mode for SD-connector-equipped Bluetooth, Wi-Fi, camera, and other adapters and was therefore usable only with memory cards.

The photo does not show the passive touchscreen display on the backside of the system board. At the time of its introduction, the iPaq was notable for the ability to view its front-lit, reflective LCD in bright sunlight; competitors' PDAs employed backlit, transmissive LCDs. Modern Pocket PCs incorporate transreflective (also known as transflective) LCDs, which combine the best attributes of both earlier generation technologies: an adjustable-intensity backlight for dim, ambient-light use and front illumination for high-ambient-lighting environments.



The iPaq 31xx, 36xx, 37xx, and 38xx product variants all employed a common processor foundation: Intel's (www.intel.com) StrongARM SA1110 CPU, running at 206 MHz. Near the CPU is an HTC (High Tech Computer, www.htc.com)-labeled ASIC, which likely acts as glue logic between the CPU and the system's memory and various input and output modules: a touchscreen display, buttons and a joystick pad, expansion buses, and an infrared transceiver.

The iPaq 3835 integrated a ROM-code-stickered, 32-Mbyte NOR-flash memory and a 64-Mbyte DRAM. The PDA directly executed the OS and factory-installed applications from nonvolatile memory. Unused flash-memory blocks found use as a user-accessible read-and-writeable "iPaq File Store" embedded drive, which a firmware upgrade would wipe clean, and user-installed applications went into system RAM. The latest generation Windows Mobile 5 OS migrates to a different memory model, which broadens the number of flash-memory options—NAND, for example—available to designers.

Although the 3835's feature set pales in comparison with today's devices, the device's bottom-edge connector accomodated a series of add-on options, such as PCMCIA and CompactFlash adapters, cameras, keyboards, and even supplemental batteries.

RAQ's

Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

The Long Term Stability of Precision Analog ICs, or How to Age Gracefully and Avoid Sudden Death

Q. *The life expectancy of my product is 20 years. How well will its calibration survive?*

A. Quite well, actually. Provided you protect it from abuse.

I am, alas, too fond of good one-liners. When asked how precision analog ICs age I usually answer "gracefully" or "365 days per year". But although these answers *are* true they are not always very helpful.

Precision analog ICs are very stable devices. Unlike wine they do not actually improve with age, but typically they have long-term age-related changes of around 1 ppm/thousand hours (the value may be given on the data sheet). It is important to realize that this aging is not cumulative, it obeys a "drunkard's walk" law. If you want the mathematics of a drunkard's walk you should consult this reference[1], but essentially each consecutive step is in a random direction. For a one-dimensional drunkard's walk this means that the distance from the origin is approximately proportionate to the square root of the number of steps.

So if a device ages at 1 ppm/1000 hours it ages at $\sqrt{2}$ ppm/2000 hours, etc. Since there are 8766 hours in a year (on average, 8760 in a normal year and 8784 in a leap year) 1 ppm/1000 hours = 2.96 ppm/year = 9.36 ppm/decade and 13.24 ppm/2 decades.

This does not vary much between devices that are continually powered, in storage, or have a reasonable range of ambient temperatures. Since this is a statistical process the variation between devices will be as large as the effect itself. High temperatures do accelerate the process, but not by very much, and the characteristics vary with different processes. Unless your circuit is spending the majority of its time above 100°C it is not unreasonable to expect aging to be close to the data sheet rate.

However there is another mechanism that causes ungraceful and abrupt changes of accuracy, and may also increase the rate of subsequent aging. That is electrostatic damage (ESD). It is a popular superstition that ESD is sudden death to an IC and that is often true. A discharge can do a small amount of damage which does not destroy the device, but does affect its performance (and may lead to sudden death later on). Such damage is often one-off but it can be cumulative—we once had a Finnish customer who complained that one of our op-amps got noisier with the passing years. Closer investigation revealed that actually nothing much had happened during the passing Summers, but it had indeed got noisier around the turn of each year, when the cold dry air of a Finnish Winter encouraged much more static electricity.

Adequate ESD protection is essential if an IC is to age gracefully.

[1] http://en.wikipedia.org/wiki/Random_walk

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BRIEF

Complete battery-pack design for one- or two-cell portable applications

By Michael Vega • Portable Power Management Applications

Introduction

Although voltage measurement alone has been used in many portable products to approximate the remaining capacity of the battery, this method may have an error rate of up to 50%. The relationship between cell voltage and capacity will vary as a function of discharge rate, temperature, and cell aging.

With the growing demand for products with longer run times, system designers need a more accurate solution. Using a gas-gauge IC to measure the charge that enters or leaves a battery will provide a much better estimate of battery capacity over a broad range of application power levels.

Gas-gauging principle

A good gas gauge requires at a minimum the means to measure battery voltage, pack temperature, and current; a microprocessor; and a proven gas-gauging algorithm.

The bq2650x and bq27x00 are complete gas gauges that have an analog-to-digital converter (ADC) for voltage and temperature measurements, and another ADC for current and charge sensing. These gas gauges also have an internal microprocessor that runs Texas Instruments' gas-gauging algorithms. These algorithms compensate for self-discharge, aging, temperature, and discharge rate in lithium-ion cells. The microprocessor frees the host system processor from constantly making these calculations.

The gas gauges have information such as Remaining State of Capacity, and the bq27x00 family provides Run Time to Empty. The information is available any time the host queries. It is up to the host to notify the end user of the battery

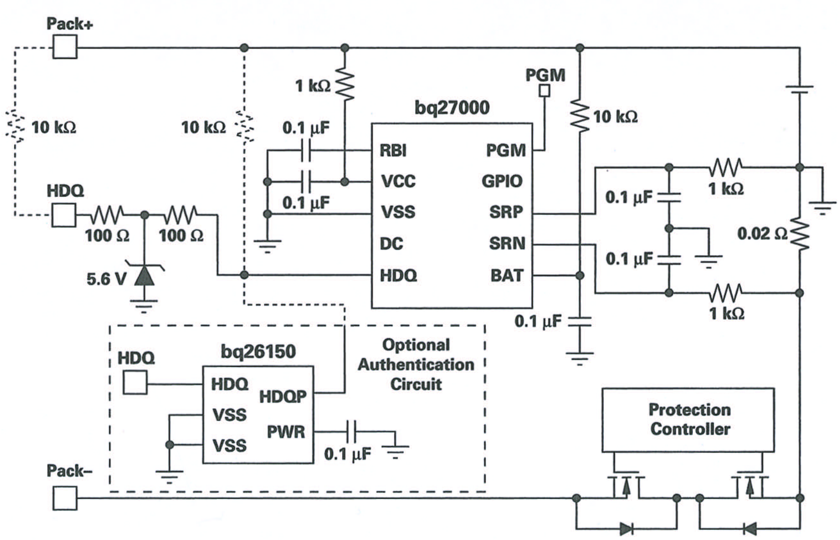


Figure 1. Typical battery pack with optional authentication IC

information either by means of LEDs or messages displayed on a screen. Using the gas gauges is very easy, as the system processor needs only an I^2C or an HDQ communication driver.

Battery-pack circuit description

Figure 1 depicts a typical application circuit within the battery pack. The battery pack will have at least three to four external terminals available depending on which gas-gauge IC is used.

The VCC and BAT pins will tap into the cell voltage for IC power and battery-voltage measurement. A low-value sense resistor is placed at the ground end of the battery cell so that the voltage across the sense resistor can be monitored by the gas gauge's high-impedance SRP and SRN inputs. The current through the sense resistor helps determine the amount of energy that has been charged to or discharged from the battery. When selecting a sense resistor value, the designer must consider that the voltage across it should be no more than 100 mV. A resistor value that is too low may introduce errors at low currents. A board layout must ensure that the connections from SRP and SRN to the sense resistor are as close as possible to the sense resistor's ends; i.e., they are Kelvin connections.

The HDQ pin requires an external pull-up resistor. The resistor should be on the host or main application side so that the sleep function of the gas gauge is enabled whenever a battery pack is disconnected from the portable device. A recommended pull-up resistor value is 10 kΩ.

Battery-pack authentication

There is an increasing problem where cheap counterfeit replacement batteries may not have the safety and protection circuits required by the original equipment manufacturer. Therefore, a battery pack may include an authentication feature as shown in Figure 1. The host challenges the battery pack, which contains an IC (TI's bq26150) that calculates a cyclic redundancy check (CRC). This CRC is based on the challenge and the CRC polynomial secretly defined within the IC. The host also calculates the CRC and compares values to determine if authentication is successful.

Once the battery is authenticated, the bq26150 is given a command to ensure that all communication through the data line is relayed between the host and the gas gauge. The whole authentication process must be repeated upon disconnection from and reconnection to the battery.

Two-cell applications

Figure 2 shows a typical application circuit for supporting two Li-ion cells with the bq26500. An adjustable voltage regulator is added for multicell support. The BAT pin of the gas gauge is connected to the positive side of the bottom cell for a scaled battery-pack voltage measurement.

The host is required to interpret the scaled pack voltage measured by the gas gauge to determine the end-of-discharge threshold and charge termination. Information such as Remaining State of Capacity can be used as it is reported by the gas gauge.

Conclusion

The bq2650x and bq27x00 gas gauges provide battery manufacturers a simple alternative for estimating battery capacity that is more accurate than just measuring cell voltage. The gas gauges can be used in different configurations, permitting authentication features and operation within two-cell applications.

Related Web Sites:
power.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with bq26150, bq26500, bq27000, bq27200, or tps71501

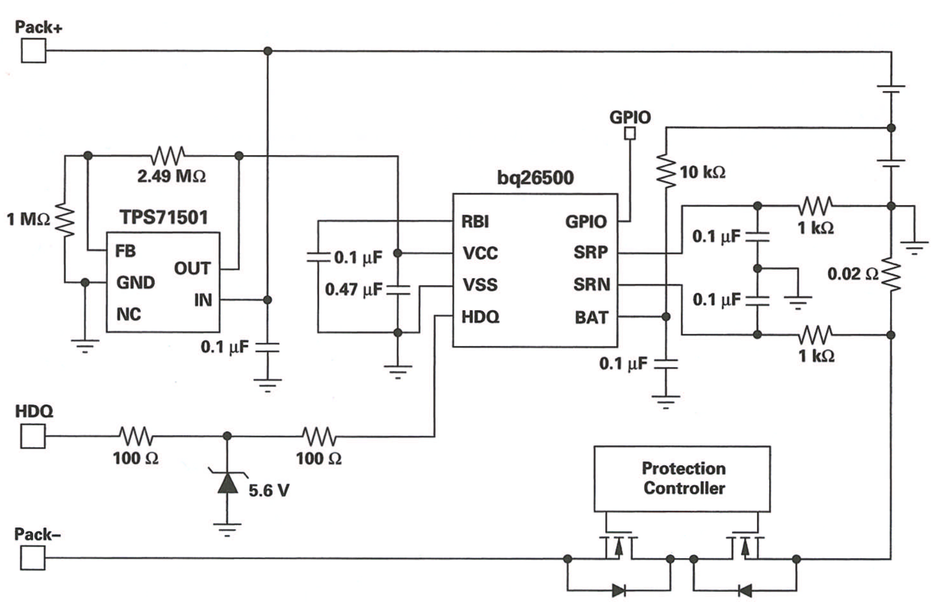


Figure 2. Two-cell application with bq26500

CONSUMER-ELECTRONICS DEVELOPERS FACE A HOST OF CHALLENGES WHEN DESIGNING FOR SMALL, PORTABLE-SYSTEM APPLICATIONS.

DISPLAY OF POWER:

PORTABLE DEVICES GET BIGGER SCREENS WITHOUT BIGGER BATTERIES

BY NICHOLAS CRAVOTTA • CONTRIBUTING TECHNICAL EDITOR

The ready availability of high-resolution color LCDs in high-end cell phones and handheld media players has changed the landscape of consumer electronics by raising user expectations for display quality in portable devices. Meanwhile, the increased use of data and multimedia services requires that displays be active more often—that is, the backlight must be on so that users can see the display—driving the relative power consumption of displays from perhaps a mere 10% of overall power consumption to, in many cases, more than 50% of the available power budget. Additionally, developers need to increase the luminescence of displays to accommodate the wide dynamic range of multimedia content. The technology sufficient for displaying text simply does not produce appealing images.

As a result, LCDs have become second in power consumption only to radio transmitters in cell phones and hard-disk drives in portable media players. In addition, higher quality displays increase BOM (bill-of-materials) costs and require more intense backlighting. Additionally, the number of pixels that a system must process and feed to the display increases interface width and frequency.

Although recent advances in battery technology have increased the overall power available to portable devices, developers cannot depend only on new innovations from this front to accommodate rising power budgets. To remain competitive, engineers must seek increased power efficiencies by taking advantage of the latest LCD technologies and carefully balancing the trade-offs between display cost, power, and size.

BIGGER NOT ALWAYS BETTER

Although consumers demand higher resolution displays, these displays are not always what they need or truly want. Higher resolution displays have lower available brightness than low-resolution displays but are more complex to design and, thus, cost significantly more. Additionally, the higher the resolution, the more power the display consumes and the wider the data interface required to the LCD. Old passive matrices, which must hold each pixel at the appropriate color, begin to consume too much power as resolution increases. Active matrices use a switching matrix to hold the value of pixels. Unfortunately, this matrix comes at the expense of reducing the pixel-to-aperture ratio and requiring a more intense backlight. Deciding which LCD process to use is difficult, especially if you consider OLED (organic-light-emitting-diode) displays and the myriad other display technologies researchers are developing, including LTPS (low-temperature-polysilicon) and PLED (polymer-LED) displays.

High resolution also drives the need for wider interfaces, which introduce physical challenges in implementing hinged designs, such as cell phones and laptops, in which computational resources reside separately from the display. High-resolution displays also require special connectors that can pass the 60 to 80 wires in a cell phone, for example, through the hinge and offer sufficient mechanical reliability.

Depending on the resolution of the display and the frame rate, a significant amount of data can be passing through a hinge at a high enough frequency to result in screen flicker. Additionally, if the interface uses TTL signaling, a significant loss of dynamic current will occur, along with enough EMI to require an EMI filter. For applications in which EMI is a problem, LVDS (low-voltage-differential signaling) can provide a means for reducing the number of wires and eliminating EMI. For example, you can aggregate an LCD interface requiring 16 to 18 wires into a single four-wire LVDS channel. For small displays, LVDS may represent overkill because some small displays' connectors have a fine enough pitch to provide a reliable connection.

AT A GLANCE

- Today's displays may consume more than 50% of the available power budget for portable-system applications; the display's backlight is responsible for most of that power consumption.
- Higher resolution displays have a lower pixel-to-aperture ratio and therefore require a more intense backlight, increasing cost and overall power consumption.
- Emerging display technologies offer innovative ways to increase display brightness and contrast without consuming more power.
- Display selection is truly a system-level decision, balancing trade-offs across all layers of development.

Part of the challenge in selecting a display technology is in determining the typical operating conditions in which the display will find use. Designing for typical use, however, may not be feasible because even a device that will find use primarily indoors and under fluorescent lights will need to provide reasonable quality when you use it outside in bright sunlight or at night. Although you should target the design for the most common case, extremes may dictate final display-technology choices and trade-off balances.

UP-FRONT ON BACKLIGHTING

The backlight consumes the most power within the display subsystem. Backlighting plays a critical role in balancing the brightness and the contrast of the display. A primary challenge that arises with a high-resolution color display is that, the higher the resolution is, the more inefficient the display becomes. The aperture ratio of a display—that is, the proximity of the pixels to each other—determines how much emitted light a user can see from an LCD. The LCD has already experienced losses in visibility due to the gaussian distribution of light over a cone; the wider the viewing angle, the larger the cone, and the less light that hits the eye from any angle (**Figure 1**). As resolution increases, the aperture ratio, along with efficiency, decreases. Additionally, color filters and polarizers that are part of the display also absorb light. To reduce the power drain of the backlight, more light needs to get from the back of the display to the front. You achieve this goal by balancing the brightness and the contrast of the display and by deploying filters and films. For example, as the contrast increases, it becomes more difficult for the human eye to differentiate between contrast and brightness. Engineers can exploit this failing because high contrast lets them use a less bright display, reducing overall power consumption.

Two primary supplemental-backlighting technologies now in widespread use are CCFTs (cold-cathode-fluorescent tubes) and LEDs. The state-of-the-art technology, CCFT, commonly finds use in laptop computers on the top and the bottom of the LCD panel. Light guides shape CCFT-emitted light to maximize its focus and, therefore, brightness across the panel. CCFTs offer consistent brightness across the entire panel. The use of LEDs instead of CCFTs is gaining in popularity. A row of LEDs along the edge of a display

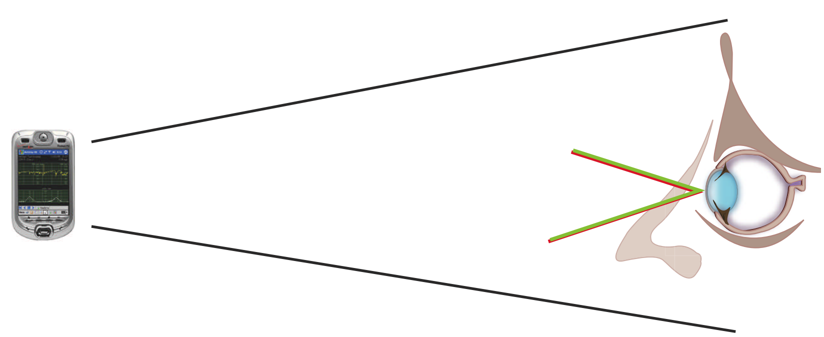
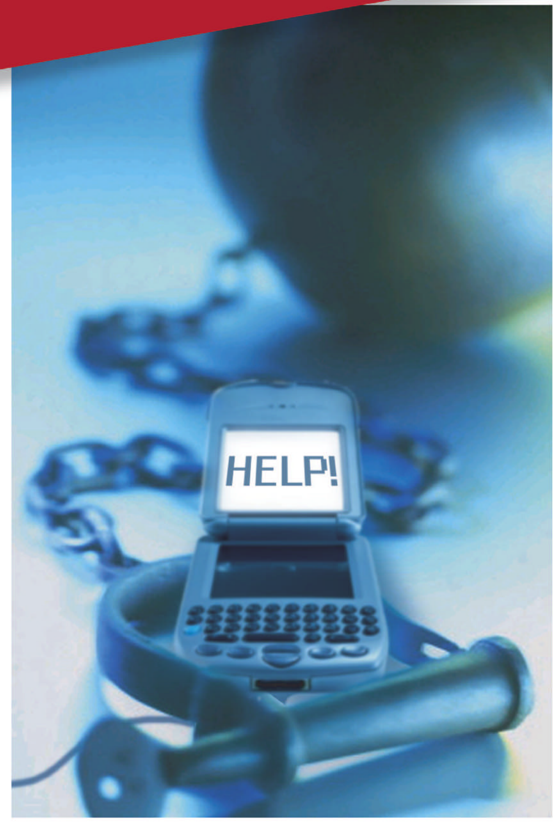


Figure 1 Losses due to the gaussian distribution of light over a cone contribute to the inefficiencies of displays, as do pixel-aperture ratio, color filters, and polarizers.

Unshackle Your Handheld Device



Intersil's ISL6299A is a fully integrated low-cost Li-ion or Li-polymer battery charger that accepts both USB port and desktop cradle chargers.

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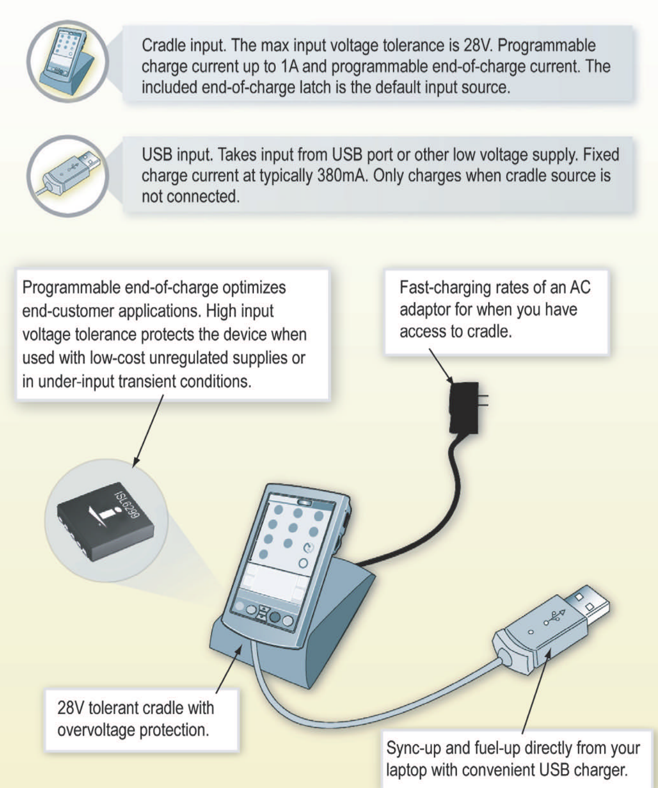
ISL6299A System



ISL6299A Key Features:

- Dual-input charger for single-cell Li-ion/polymer batteries for cradle and USB
- Low component count
- Integrated pass element
- Fixed 380mA USB charge current
- Programmable cradle charge current
- Charge current Thermaguard™ for thermal protection
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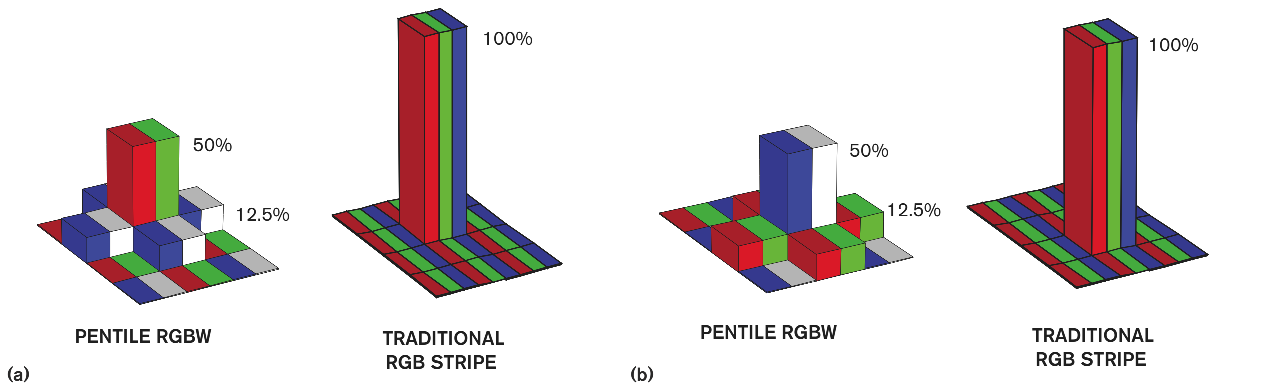

Figure 2 Clairvoyante's PenTile technology uses an RGBW-based approach that pairs pixels rather than use triplets to achieve equivalent resolution to that perceived by the human eye. The use of alternating red/green and blue/white pairs increases the aperture ratio, and the presence of a white subpixel allows more of the available light to pass through. The pixel is located at the second row, second column (a) and at the third row, second column (b). Subpixel rendering uses neighboring subpixels across a 3×3 matrix to eliminate moiré or aliasing artifacts.

provides a backlighting source that is brighter and more power-efficient than a CCFT. Developers can either offer significantly greater brightness for the same power as a CCFT or the same brightness with less power. However, they must take care when using LEDs, especially with smaller displays, such as those in cell phones, because LEDs offer a point source of light, and brightness varies depending on the distance and overlap between LEDs. LEDs are also more expensive than CCFTs.

One important disadvantage of CCFTs is that they generate heat multidirectionally in a sphere away from the tube. This fact can make it difficult for the CCFT to dissipate heat as it warms during use; instead, it must passively dissipate heat because the use of a fan is impractical. As a consequence, a CCFT loses as much as 20% of its brightness after one hour of continuous operation. Contrast this situation with that of LEDs, which generate heat primarily in one direction. Through the use of specialized heat-sinking techniques, you can wick away heat from LEDs so that they will lose perhaps only 10% of their brightness after running for 15 hours. LEDs also are rugged because, as solid-state components, they are less susceptible to physical damage.

Heat is an important limitation in the design of an LCD, especially one for industrial and military applications. LCDs use a liquid that may operate improperly at high or low temperatures. Additionally, backlights typically require an inverter. You can reduce thermal issues by placing the inverter and the LCD on separate pc boards and placing the inverter close to the edge of the box.

Achieving the highest power efficiency requires designing a screen that users can frequently view without the use of the backlight or with a dimmer backlight. For devices that find use in a variety of operating environments, a variable backlight can increase overall power efficiency. For example, you can set a variable backlight to 0, 50, or 100% intensity, depending on the available ambient light. In this way, you need not provide an excess of power to the display to accommodate extreme operating conditions when the display is working only in more common, everyday applications. You can set the intensity of the backlight using a light sensor, but this approach might prove too power intensive, costly, and complex to implement in consumer applications. A more practical approach would be to base intensity selection on user profiles. For example, when a user talks into a cell phone, as long as the phone is not in speakerphone mode, the user is not looking at the screen. In this case, you can not only turn off the backlight, but also reduce the number of screen updates that occur. Additionally, LCD drivers can often work in different modes. If the screen is displaying a static image, such as a map or a photo, the screen requires less frequent frame updates.

FILMS, FILTERS, FORM FACTORS

Other ways to improve brightness are to use optical bonding techniques and different filters. CI Lumen, for example, improves the contrast of commercially produced panels through a number of technologies. Alternatively, you can replace CCFTs with LEDs to increase brightness or replace films or filters inside the LCD with higher quality films that increase transitivity. Typically, LCD manufacturers base filter selection not on which filters are the most efficient but on which are the most cost-effective choices across their customer base. For applications in which power efficiency is more important than cost or size, such as in marine, aviation, and military applications, replacing films and filters becomes a viable option.

In addition to adjusting films and filters, you can add an extra antireflective-coating glass, antiglare coating, or both on the front surface of the display glass. You can optically bond this glass to the LCD to eliminate the air gap between the LEDs and the face of the LCD. This approach improves the transitivity of the LEDs and reduces undesirable reflections from the back of the glass. This stage is important because increasing brightness without improving contrast results in a display that appears bright—but also washed out—in sunlight. In reality, users can't see the display in sunlight because of low contrast, not low brightness.

Using optical bonding cannot be a last-minute decision because it adds to the thickness of the display. Optical bonding typically adds approximately 20% to the cost of a display panel,

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making it an option for applications in which brightness or power consumption is the primary design consideration, such as for mobile tablet computers, PDAs, or industrial sensors.

Another alternative is to use RGBW (red/green/blue/white)-based technology, such as the technology that Clairvoyante licenses to LCD manufacturers. Clairvoyante breaks pixels into pairs rather than triplets (**Figure 2**) and achieves an equivalent resolution to what the human eye perceives. The use of alternating red/green and blue/white pairs increases the aperture ratio, and the presence of a white subpixel allows more of the available light to pass through. Additionally, innovative subpixel rendering uses neighboring subpixels across a 3×3-pixel matrix, fine-tuned through second- and third-order adjustments, to eliminate any moiré or aliasing artifacts. The overall result is a doubling of LCD transitivity, giving engineers the option of halving backlight intensity to achieve the same white luminescence for the same power.

Developers also have the option of switching to new display form factors, such as microdisplays from companies such as Kopin. These displays have made significant inroads as camcorder viewfinders and in military applications, such as night-vision goggles and weapon sights. Microdisplays have begun to find traction in mobile video applications in which they can offer a perceivably large, 0.97-in.-diagonal display with resolution of 1280×1024 pixels. That is, although the screen is small, it is so close to the eye that it fills the field of vision, providing the equivalent experience of a 48-in. monitor viewed at a distance of 7 feet. It is important to note that long-term viewing of a single microdisplay is taxing to the eye, necessitating the use of two displays. Prices for ¼-VGA-resolution microdisplays start at $10 (low volumes).

SURFACE CONSIDERATIONS

Evaluating trade-offs for selecting a display can be difficult. Consider the details behind implementing an LED-based backlight. After deciding to use LEDs rather than CCFTs, developers have the option of configuring LEDs in parallel or in series, because one driver can drive several LEDs. If you drive them in parallel, you'll need four times more current to light four LEDs than you would need if you drove them in series. Running them in a parallel configuration also requires four wires, which can consume additional conductors in the power ribbon cable. Another disadvantage of a parallel configuration is that the brightness of an LED is relative to the current passing through it. Hence, to achieve a consistent backlighting source, the current through each LED must match that of the other LEDs within a few percentage points.

Alternatively, running the LEDs in series requires only one wire and provides a single current through all LEDs for better brightness matching, but, in this case, you must boost the voltage. Four white LEDs in series operating at 4V each can require a voltage as high as 18V, in turn requiring an inductive boost of the system voltage. Inductors, however, increase cost and consume board space as well as increase EMI emissions. EMI reduces the sensitivity of radio subsystems, so you must employ a more expensive inductor or another measure in applications such as cell phones.

Because they keep the voltage under 6V, parallel implementations can use switch capacitors to boost a system voltage to 4V from 1.8 or 3V to drive the white LEDs. Switch capacitors are cost-effective and generate no EMI, but they have typical efficiency of only 75%. To improve efficiency, developers can use synchronous boost converters, which replace the internal Schottky diode of asynchronous converters with a PFET. For even higher efficiency, developers can employ a multimode switched capacitor that can boost voltage by a factor of two, one and one-half, or one—that is, without boosting. This approach enables more efficient boosting as battery voltage drops during normal discharging. For example, you can boost a 4.2V lithium-ion battery at full charge times one to provide the necessary 4V. As the battery drops below 4V, the switched capacitor can shift to a one-and-one-half-times boost to provide 5V from 3.6V. Later, as the battery drops to 2.8V, the switched capacitor boosts at two times to provide 5.6V. If the switched capacitor offers only dual-mode operation—that is, one- and two-times boosting—the LEDs will boost to two times as soon as the battery drops below 4V, resulting in higher inefficiencies and losses.

There is no simple answer for whether to drive LEDs in series or in parallel. Optimizing backlighting power efficiency is like a fairly complex equation that you must solve, with the various variables representing cost, efficiency, size, and complexity. To achieve the highest efficiency, you need to evaluate display trade-offs across all layers of development—from the base silicon to supporting power circuits and from interface lines to actual usage, as the application determines. You cannot isolate the individual layers from each other.

For these reasons, selecting a display comes early in the design process, usually at the same time that you select the primary processor and operating system. Display selection is truly a system-level decision that has significant impact on other design decisions. Fortunately, developers have a multitude of options available to them so that they can achieve an implementation that enables them to improve the user experience through higher resolution without adversely increasing battery size, system cost, or device form factor. **EDN**

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AUTHOR'S BIOGRAPHY

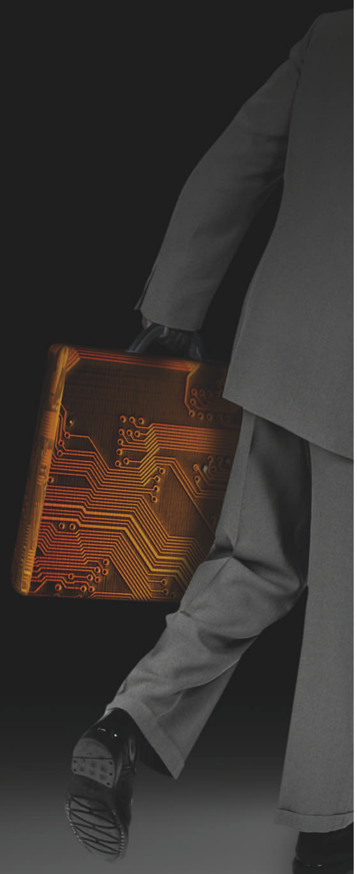
Contributing Technical Editor Nicholas Cravotta just celebrated the issuance of his latest patent. He is currently developing an innovative accessory for the video iPod.

LOW-COST KITS: THE NEW FPGA-DESIGNER TREND

DOMINATING COMMUNICATIONS AND COMPLEX INDUSTRIAL APPLICATIONS, FPGA MAKERS ARE LOOKING TOWARD DESIGN WINS IN LOWER END AUTOMOTIVE AND CONSUMER DEVICES. WITH TODAY'S DEVICES BLURRING THE DISTINCTIONS BETWEEN CPLDs AND FPGAs, LOW-COST DESIGN KITS HELP FIRST-TIME USERS TACKLE SOPHISTICATED SYSTEMS.

BY DAVID MARSH • CONTRIBUTING TECHNICAL EDITOR

In the 1970s, low-density and power-hungry TTL packages filled every digital designer's schematics. But, before long, silicon architect Ron Cline at Signetics developed the world's first PLA (programmable-logic array)—a device that could pack multiple TTL functions on a single chip by configuring fuses between its AND-OR gate planes. Since that time, programmable logic has evolved to the point that today's FPGAs (field-programmable gate arrays) routinely furnish as many as 10 million gates to address complex applications, notably within the communications infrastructure. And there's no sign of any slowdown in this burgeoning market; market-research company In-Stat estimates that the $1.895 billion 2005 FPGA market will balloon to $2.7567 billion by 2010 (**Reference 1**).



Furthermore, the company believes that the largest user groups will continue to be communications and industrial sectors, growing from 73.8% in 2005 to 76.8% by 2010.

Given this focus, it's unsurprising that many designers perceive programmable-logic devices as difficult to use, expensive, and power hungry. But at the lower end of the spectrum, the silicon vendors are making a concerted effort to secure design wins within the automotive and consumer markets. As *EDN* recently reported, part of this drive consists of producing lower-gate-count devices with the lowest possible power consumption to enable use in portable electronics and "always-on" automotive applications (**Reference 2**). But what does it take for a potential user to get started using low-end programmable silicon in terms of approachability and ease of use, future extensibility to suit target applications, and cost?

With these considerations in mind, *EDN* assembled a selection of low-cost development kits that support in-system-reprogrammable devices. Such devices are the natural choices for prototyping, as well as for production applications, when the ability to perform field upgrades can provide a competitive advantage. Given volume pricing of around $1.50 for entry-level devices, cost is no longer a barrier to using reprogrammable logic—and evaluation kits are available for as little as $49. So what do you get for your money and how easy is it for a novice to use?

300,000 GATES

Costing approximately $285, Actel's ProASIC Plus starter kit contains a 134×125-mm evaluation board that carries the company's 300,000-equivalent-gate APA300 FPGA surrounded by a mass of headers that make available every device pin. Various jumpers enable, for instance, an array of eight user LEDs, and five pushbutton switches provide user input. A high-density, 26-pin header connects to the accompanying FlashPro Lite programmer, which a parallel-port cable links to a host PC. A universal-input ac-line adapter provides 9V dc that a pair of TPS776xx voltage regulators downconvert to 2.5 and 3.3V levels. The chip's core requires 2.5V, and jumpers select 2.5 or 3.3V for the I/O blocks. The starter-kit CD includes a user's guide and resources such as schematics and design files that complement the printed *User's Guide & Tutorial*. Two further CDs furnish the Libero IDE (integrated design environment) and Logic Navigator debugging software. Usefully, the board's FPGA comes preprogrammed with a test program that confirms hardware operation.

Like other ProASIC Plus family members, the APA300 is built in an "instant-on," reprogrammable flash technology that dispenses with external configuration memories and their support logic. The chip's architecture uses a "sea-of-tiles" fabric that's surrounded by embedded dual-port SRAM modules and a package-dependent number of I/O pins. With the exception of a three-input XOR gate, it's possible to configure each of the APA300's 8192 tiles as a three-input, single-output logic function—such as a D-type flip-flop—and connect it with others using the chip's routing resources (**Figure 1**). Available routing options are local, long line, very long line, and global. Of these, local is the fastest and allows a tile's output to connect to every input of its eight neighbors in a nine-tile array. The long-line resources run horizontally and vertically across the device and can span one, two, or four tiles. The very-long-line resources similarly cover the device in a grid pattern to suit high-fan-out nets, and the global resources typically suit clock and reset-line distribution. Other distinguishing features include programmable Schmitt-trigger inputs on each I/O pin, together with two clock-conditioning blocks that comprise an analog phase-lock loop, delay lines, a quadrature phase-shifter, and clock multipliers and dividers. A clock-tree network built from spines and ribs that reach every tile within their respective regions permits the APA300 to efficiently distribute as many as 32 clocks.

Promising start-to-finish design-flow guidance and control for novice and experienced users, Libero's default installation occupies slightly more than 1 Gbyte of disk space. The software runs under Windows 2000 Pro SP4/XP Pro SP2, Sun's Solaris, or Red Hat's Linux. Following installation, Web-site registration results in the arrival of an e-mail that contains a license file for the Gold IDE edition that node-locks the installation to the PC's hard disk. Crucially, this file also enables the Synplicity Identify AE (Actel edition) software components. Running the IDE then checks the Web for updates—in this case, offering a 443-Mbyte self-extracting archive that contains Version 7.2, plus 56 Mbytes more of Service Pack 2. Because the download is a complete copy of the IDE that requires you to uninstall the original or install it in another directory, you may wish to ignore the CD in favor of the Web package. Download and read the IDE's *Quick Start Guide* while the procedure completes.

AT A GLANCE

- Programmable devices target automotive and consumer markets.
- Midrange devices blur traditional CPLD/FPGA (complex-programmable-logic-device/field-programmable-gate-array) definitions.
- Low-cost development kits promise to speed design.
- Accessibility is the key to complex software-tool environments.

The tutorial starts off with compiling an AND gate in VHDL (very high-speed-IC hardware-description language), neatly demonstrating the step-by-step discipline that Libero enforces (**Figure 2**). Users who are new to VHDL and its popular alternative, Verilog, can find a great deal of introductory material on the Web. (See **references 3** and **4** for Verilog-specific links and similar VHDL resources, respectively.) The power of these design-entry tools instantly becomes clear when you're attempting something as simple as a 16-bit counter—although the schematic-entry route traditionally requires you to replicate each flip-flop and all of its connections, modifying a few parameters within a standard VHDL text file allows you to build a counter of arbitrary length.

Because it's easy to get lost within some environments, Libero's sequential procedure is a boon to new users without being too prescriptive for regular use. Sadly for users, a typo in the library package reference causes your very first VHDL compilation to fail: The "iee" in the third line should read "ieee." Fix this glitch, and the next step runs SynaptiCAD's WaveFormer Lite, a subset of the $2500 WaveFormer Pro tool that generates test-stimulus data from graphical inputs. You can also create the testbench data directly within Libero's HDL (hardware-description-language) editor. Right-clicking the andgate.vhd sample file offers options that differ from the tutorial—which was written around Libero Version 2.3 SP2—yet this step and later ones that differ are easy to transpose. Selecting Run Presynthesis Simulation offers the opportunity to associate the stimulus file with andgate.vhd; accept this option, and the Actel version of Mentor Graphics' ModelSim launches to compile the stimulus data. Among the mass of information that floods the screen is a waveform window that displays the A and B inputs that you created in WaveFormer Lite, as well as the simulator's logical output of these two signals.

Having verified that the design works correctly, you next generate an EDIF (electronic-design-interchange-format) netlist file using Synplify. Libero seamlessly translates the resulting output file into a VHDL netlist, which then appears within the IDE's file-manager window. If any errors occur, you can edit the file within Synplify, which back-annotates changes to Libero. Running a post-synthesis simulation in ModelSim now displays the output waveform, including propagation delays. To implement the design, run Designer, select the device and its package, and click Compile. When this button turns green—signifying successful compilation—assign the AND gate's pins by drag-and-drop within Pin Editor, run Layout and Back-An-

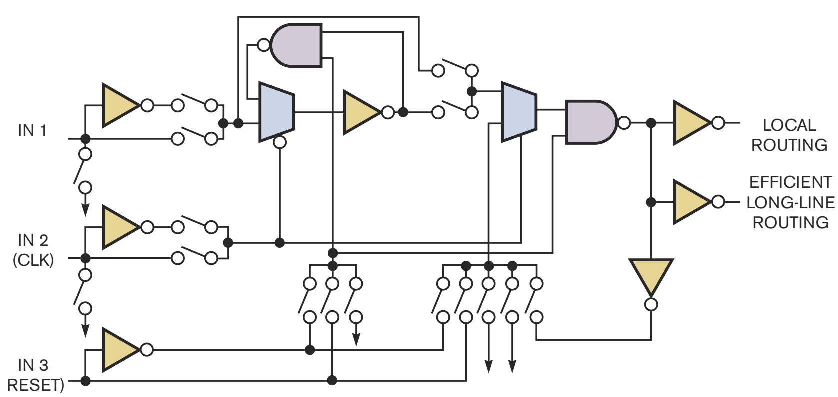
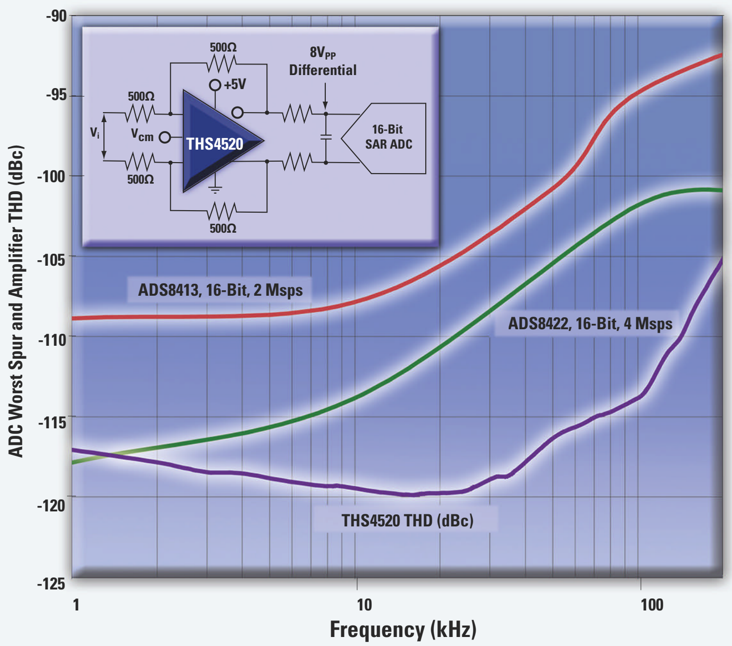


Figure 1 Except for a three-input XOR gate, each tile in Actel's ProASIC devices can accommodate any three-input, one-output function.

Lowest Distortion, 16-bit Differential ADC Driver



The **THS4520** from Texas Instruments is a wideband, fully-differential op amp with rail-to-rail output. The independent output common-mode control makes it well-suited for dc-coupled, high accuracy data acquisition systems. With its low distortion, the THS4520 is ideal to drive TI's industry-leading, 16-bit SAR data converters.

▸ Applications

- 3.3V and 5V high-resolution ADC driver
- Wireless communication
- Medical imaging
- Test and measurement
- Differential DAC output amplifier

▸ Features

- Rail-to-rail output
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- Very low distortion:
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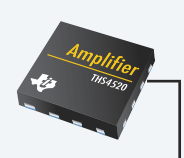
  - HD3 of –123dBc at 100kHz (8Vpp, R_L = 1kΩ)
- Independent output common-mode control
- Power down capability: 15µA quiescent current
- Pin-compatible family of fully differential amplifiers
- Available in a small QFN-16 package

Device	Supply Voltage (V)	GBW Product (MHz)	Slew Rate (V/µsec)	Settling Time 0.1% (ns)	Voltage Noise (nV/√Hz)	Supply Current (mA)	Output Headroom (V) (200Ω Load)	Min. Stable Gain (V/V)	THD (dBc)*	Price (1k)**
THS4520	5	1200	570	7.0	2.0	14.2	0.3	1	–92	$2.25
THS4508	5	3000	6400	2.0	2.3	39.2	1.2	2	–101	$3.95
THS4509	5	3000	6600	10	1.9	37.7	1.1	2	–103	$3.75
THS4511	5	2000	4900	3.3	2.0	39.2	1.2	1	–106	$3.45
THS4513	5	2800	5100	16	2.2	41.9	1.1	1	–105	$3.25

** f=10MHz, 2Vpp, 200 Ω load*
*** Suggested resale price in U.S. dollars in quantities of 1k*

For Samples, Evaluation Modules and Technical Information



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Technology for Innovators™ TEXAS INSTRUMENTS notate, and the IDE will save a file called andgate.ahb, whose timing characteristics you can again simulate within ModelSim before programming the device. The Programming File button within Designer produces a STAPL (standard-test-and-programming-language) file that it deposits within the Implementation Files section of the IDE's file-manager window. In the meantime, the IDE's design-flow window tracks each of these process steps and leaves you ready to program the device.

The details of the FlashPro 4.2 programming software differ somewhat from the printed description that relates to an earlier revision, but the steps are obvious to follow. Pressing switches 1 and 2 then illuminates LED 1 and signals correct compilation and programming of this VHDL textual example. Users wishing to explore schematic entry using ViewDraw then have to use some initiative; there is a limited amount of tutorial material on the Web site, but the main information sources lie within the user guides that the ViewDraw directory contains. It appears that this tool borrows from the Innoveda eProduct Designer suite from Mentor Graphics, which a number of documents describe—notably the "old" and current versions of the ViewDraw manual, with the former usefully including much tutorial material. Even without these resources, ViewDraw is sufficiently intuitive that it's easy to generate another gate example and redirect its output to another LED, by which time the design-flow process seems familiar.

Dennis Kish, senior vice president of sales and marketing at Actel, advises new users to consider the ProASIC3/E product family that the company introduced last year. This family spans 30,000 to 3 million system gates, packs approximately 25% more logic, and operates about twice as fast as similar ProASIC Plus devices. It includes features such as hot-swappable I/O structures that greatly ease complex board-management applications. Kish also points to the company's Fusion PSCs (programmable-system chips), which integrate analog functions such as ADCs to particularly suit system-management roles. Kish says that Actel will offer for sampling its Igloo family, which targets portable electronics

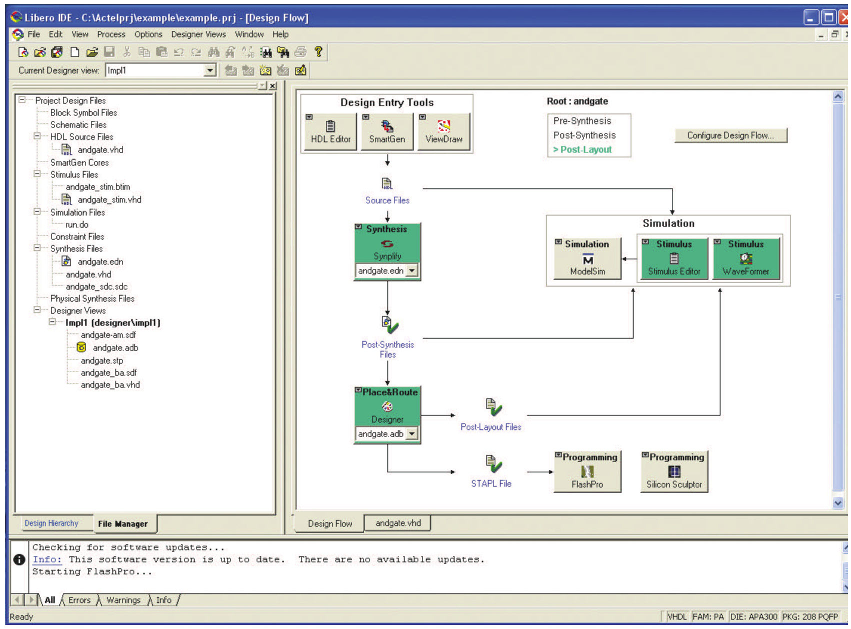


Figure 2 Libero's IDE guides users through every design and implementation step.

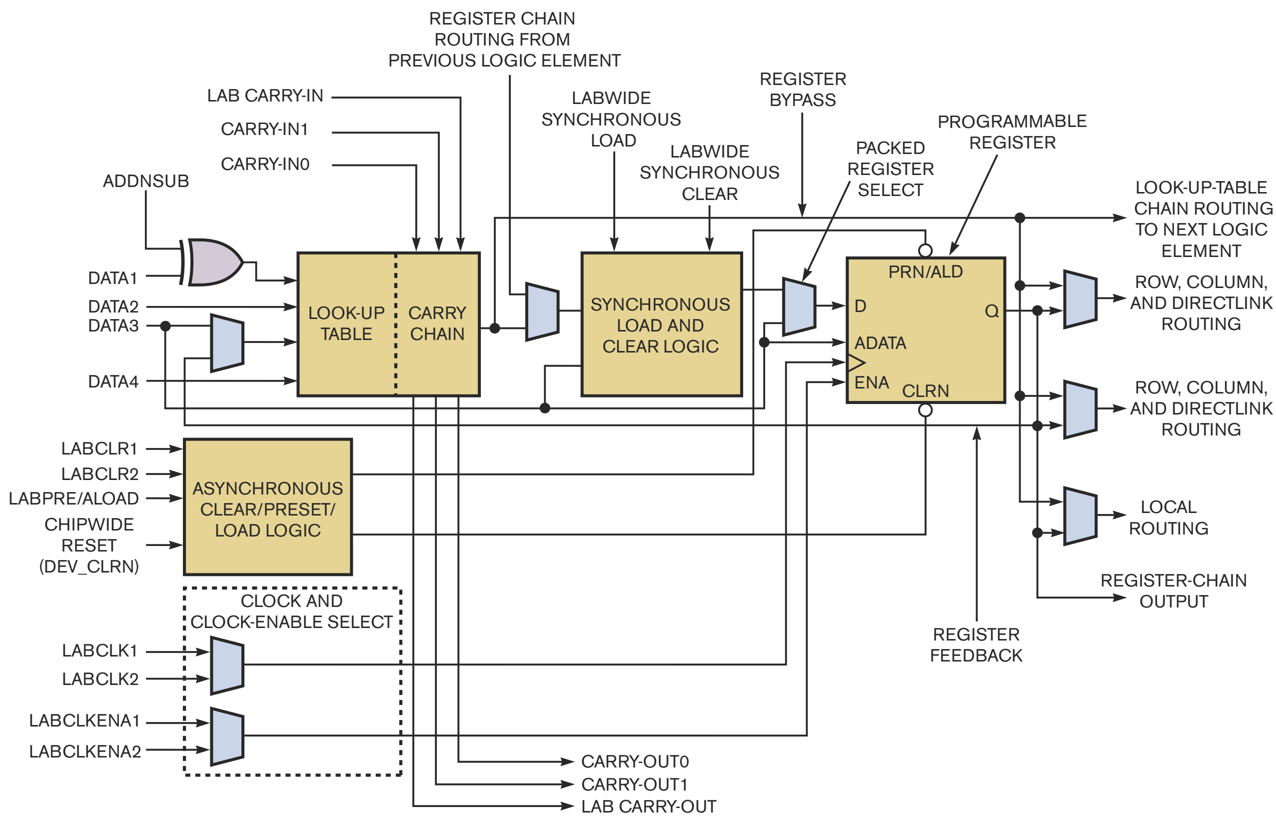
and low power consumption, in the first quarter of 2007. This new family is compatible with ProASIC3/E but includes the FlashFreeze power-save input pin, which effectively tristates the device and retains all state information. This approach reduces the power consumption for the smallest AGL030 device to approximately 5 μW.

In the meantime, because Actel is the only FPGA vendor to license the ARM7 core, the company's relationship with ARM flourishes, notably with the availability of a low-cost edition of ARM's high-end RealView suite at a price that targets the FPGA market. Over the next few months, Kish promises new reference designs to complement free tools that range from a GNU-based ARM development-tool set that he reckons is 25 to 30% less efficient than RealView—"not so important when Fusion offers half a megabyte of flash"—to IP (intellectual-property) blocks that emphasize on DSP functions: "With our tools, we've optimized our easy-to-use software for new FPGA designers and retained options and short cuts for power users," he says.

CPLDs BLUR FPGA DIVIDE

As the market leader in CPLDs (complex-programmable-logic devices) for some 15 years, Altera continues to use that term to describe its MAX II product line. The family comprises four devices with 240 to 2210 logic elements—which the company equates to typically 192 to 1700 equivalent macrocells—in packages that range from 100-pin TQFPs to 324-pin BGAs. Maximum user-I/O count spans 80 to 272 pins, and the hot-socketable devices support I/O logic levels of 1.5, 1.8, 2.5, and 3.3V. An internal voltage regulator performs the 3.3/2.5 to 1.8V downconversion necessary for the core logic. Other useful features include programmable Schmitt-trigger inputs and compatibility with the PCI (peripheral-component-interconnect) 2.2 standard for 3.3V operation at 66 MHz. (The device's maximum count frequency is 304 MHz.) The flash memory retains configuration data to enable instant-on operation, with an 8-kbit area set aside for user data.

The fact that these devices employ look-up-table architecture suggests that they have more in common with FPGAs than PLDs (see **sidebar** "CPLDs go fast and wide" at the Web version of this article at www.edn.com/061123cs). Denny Steele, senior marketing manager for Altera's low-cost products, explains that the fabric that generates



NOTE: LAB=LOGIC-ARRAY BLOCK.

Figure 3 Altera's MAX II CPLDs have more in common with FPGA logic cells.

product terms traditionally differentiates CPLDs from FPGAs: "A traditional CPLD embodies a product-term fabric that's typically built using an AND-OR array, which is just great for applications such as address decoders," he says. By comparison, FPGAs employ a four-input-look-up-table architecture that implements every logical function from effectively four address lines: "Because this design is so fast at performing arithmetic, FPGAs have naturally gravitated toward DSP and communications applications," says Steele. Another key differentiator, he says, is the CPLD's use of crosspoint-switch-routing resources that run everywhere, versus an FPGA's segmented routing, which directly and deterministically links large logic blocks.

For Altera's EPM1270 device, the hardware within the company's $150 MAX II development kit comprises the development board, a ByteBlaster II parallel-port download cable, and a USB cable for connecting the board to a PC host. The board's PCI-format outline accommodates the CPLD, a 1-Mbit Cypress SRAM, and an ADC with current-sensing circuitry to monitor the CPLD's power consumption. In addition, the board has a two-line, 16-character LCD and the usual array of LEDs, switches, and headers, together with USB and PCI interfaces. The PCI interface is 3.3 and 5V-tolerant. One CD provides a Web edition of the Windows NT/2000/XP-compatible Quartus II development software, and another furnishes system documentation, including an electronic copy of the printed *Getting Started* guide.

The EPM1270 arranges 127 LABs (logic-array blocks) into a 2-D row-and-column structure. Each LAB comprises 10 logic elements, each of which is built from a four-input-look-up-table core with surrounding control, feedback, and routing resources (**Figure 3**). Using a look-up table allows every logic element to implement any four-input function; LAB-wide carry logic enables fast arithmetic across multiple logic elements. Output signals can route directly to the next logic element, to the local and global routing system, or through a programmable register before connecting into routing resources. The design accommodates two operating modes—normal and dynamic arithmetic—that the compiler within the Quartus software exploits to best suit normal logic or arithmetic operations. A fast local interconnection system routes signals between adjacent logic elements within the same LAB, and row-and-column interconnections enable global connectivity.

Install the starter-kit material, obtain a license from Altera's Web site, and check the site for a newer version of Quartus II Web edition before installing it; in this instance, Version 6 Service Pack 1 replaces the CD's Version 5 with a 263-Mbyte download. You can optionally install an evaluation copy of Altera's PCI MegaCore IP library, which—if you decide to license the capability—is available for $1995, representing a $3000 discount for purchasers of this development kit. When installing the system software,

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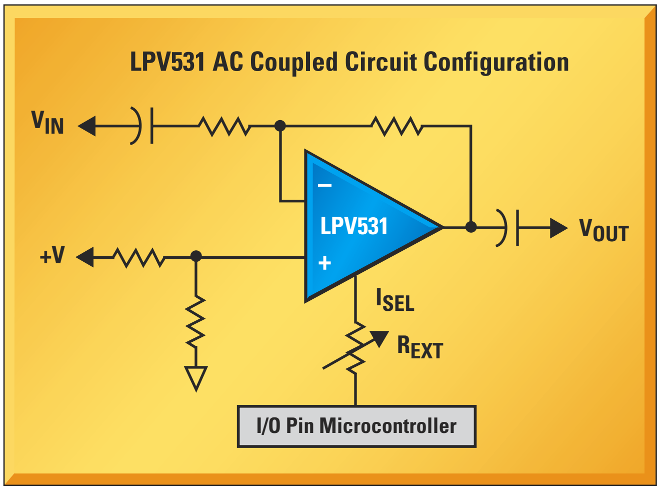

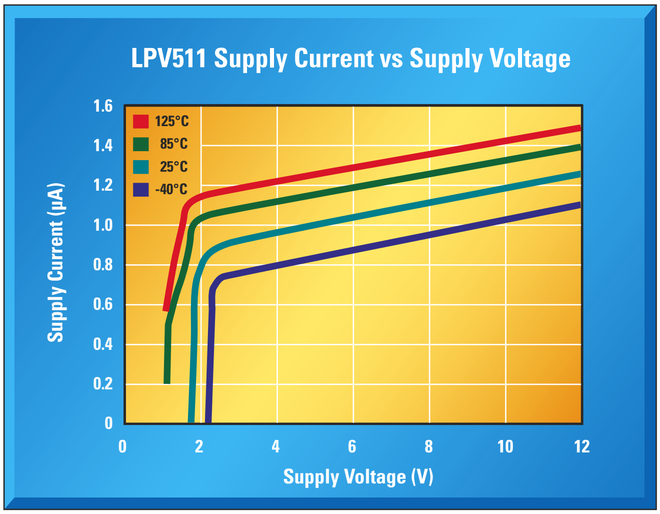

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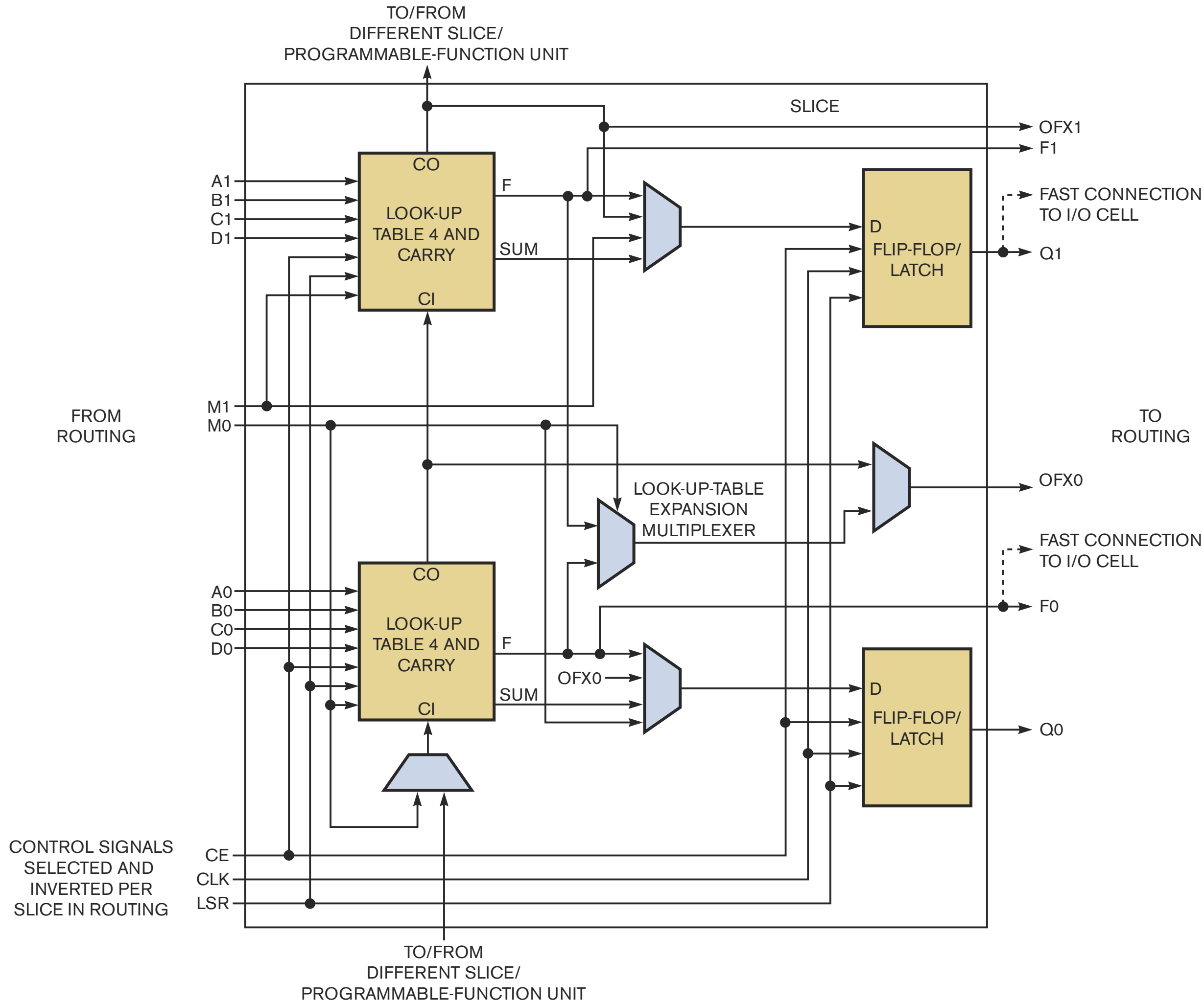

Figure 4 Each "slice" in Lattice's MachXO comprises two look-up-table functions.

be sure to select the Talkback feature, which enables the SignalTap embedded logic analyzer, SignalProbe, and FastFit facilities. It's also worth noting that, in common with all the other boards this article covers, it proved impossible to install the parallel-port programming hardware on a recent PC that has no native parallel port. No product would recognize a parallel EPP/ECP (enhanced-parallel-port/enhanced-capability-port) card that provides legacy support for printers and dongles; in this case, it returned a "no-kernel-driver-installed" message despite the driver's appearance in XP Pro's Device Manager. These issues vanished when substituting a PC with traditional LPT1 and serial ports.

In benchtop use, the MAX II board derives its power from the USB connection that jumper J8:1-2 selects. The board comes with its EPM1270 preprogrammed to run a functional test program that confirms correct hardware operation; you can also reprogram the board with this code using the ByteBlaster tool. Three more demo designs reside within the starter kit's examples\HW\demos subdirectory. They show the EPM1270's power-up timing characteristics, its power consumption, and its ability to be programmed in the background while running another code set—a facility that promises seamless dynamic reconfiguration. For instance, the low-power routine offers the ability to add 150 flip-flops at a time and vary their toggle rate with the LCD reporting current draw; the in-system programming demo allows you to load another routine as the primary code set runs. Pressing switch S_5 then interrupts the core-voltage power supply, reconfiguring the chip to run the program that you loaded in the background.

Other tutorial software includes reference designs for USB and PCI, along with a slot-machine example. Of these, only the USB example contains Verilog HDL-code sources to guide users familiar with this entry methodology. Sadly, it seems, the immediate help ends here; although the Quartus Help menu includes a step-by-step tutorial for using the IDE along with two introductory manuals for Verilog and VHDL users, the material is a poor educational tool. For instance, the IDE tutorial steps through processes without hinting at why these processes are necessary. After I spent more than two hours follow-

EXPLORING THE DIRECTORY STRUCTURE REVEALS AN EXAMPLES SUBDIRECTORY THAT INCLUDES A TUTORIAL SECTION THAT'S DEVOID OF ANY DOCUMENTATION.

ing a series of arcane steps to arrive at the compilation stage, my first experience failed with a fatal Verilog port-declaration error in the hvalues.v file, which I copied directly from the tutorial's instructions; two further attempts were no more successful. Altera's Web site reveals numerous design examples of functions that range from commonplace to exotic, but there does not seem to be a simple guide to getting started.

Users with greater aptitude, experience, or time will doubtless revel in the power that the Quartus IDE promises, such as its block symbolic entry, library primitives, and prebuilt "megafunctions," which you can use as is or customize. There's even a 74-series TTL function library from the earlier MAX-II software interface that may appeal to hardened discrete-logic fans. But for a first-time user like me, the absence of a beginner's tutorial renders the IDE impenetrable; the *Introduction to Quartus II* manual, which similarly lacks any such help, runs to more than 260 pages, and the five-volume Quartus II handbook set is a massive 2160-pg tome!

EASY MIXED-MODE DESIGN

Lattice Semiconductor's $99 MachXO starter evaluation board measures only 85×72 mm, and most of that space is for headers and connectors. The minimalist hardware comprises the LCMXO256C device in a 100-pin TQFP package, a 33-MHz oscillator, various switches and LEDs, a header for a JTAG connection, and no fewer than three power-supply regulators. These components downconvert the ac-line adapter's 5V dc to 3.3 and 1.2V for appropriate versions of the core, and an adjustable regulator allows users to set I/O-bank levels of 1.25 to 3.3V; out of the box, all levels are set at 3.3V. A printed *User's Guide* describes the board's hardware and lists I/O connections. You also get an ispDownload cable to link a PC host's parallel port with the board's 10-pin JTAG header, plus a leaflet that describes the programmer.

Unusually, the box contains no software. A single-page flyer points you toward the company's Web site as the source of the ispLever-Starter development environment that's necessary to run the system. Download your choice of software files from Lattice's Web site. At a minimum, you need the base CPLD module; the FPGA extension; and the Precision synthesis engine, the Synplify synthesis engine, or both. Then, request and install a license file, and start the software. But don't forget the separate step of installing the parallel-port driver. Also, be sure to install the Help and User Guide files, because this route furnishes the most straightforward method of becoming familiar with the environment. The recently released Version 6.0 of the IDE introduces numerous updates that include huge improvements to the Help system over the Version 5.1 that I tested earlier, so be sure to update if you have an older installation.

Exploring the directory structure reveals an Examples subdirectory that includes a tutorial section that's devoid of any documentation. In keeping with Lattice's Web-resource spirit, download the *MachXO Family Handbook* to first understand the device architecture. The LCMXO256C that the evaluation board carries is the smallest member of a family of devices offering 256 to 2280 look-up tables, 2 to 7.5 kbits of distributed SRAM, and as many as three blocks of 9-kbit embedded memory in a range of packages that support 78 to 271 I/Os. The two top-specification devices also offer one and two PLLs, respectively. Lattice refers to the MachXO family as a "crossover" device, asserting that this look-up-table-fabric architecture combines the best features of CPLDs and FPGAs to optimally suit use in low-end FPGA applications. Its nonvolatile implementation enables power-up performance within a few microseconds, and the on-chip configuration data alleviates the security concerns that accompany external memories and the possibility of decoding their bitstreams.

The architecture subdivides logic blocks into PFUs (programmable-function units) and PFFs (programmable-

function-units without RAM or ROM). PFUs contain the building blocks for logic, arithmetic, register, and distributed RAM and ROM functions, and PFF blocks suit logic, arithmetic, and ROM functions. Each block of either capability comprises four interconnected slices, each of which houses two look-up tables and their output registers, together with 14 input and seven output signals (**Figure 4**). Each slice supports four operating modes: logic, ripple, ROM, and RAM. Users can concatenate the four-input combinational look-up tables in logic mode to synthesize arbitrary-width functions. The ripple mode, a 2-bit arithmetic-logic unit, also supports counter and comparator functions. The RAM mode allows users to construct 16×2-bit distributed memories including dual-port configurations. The ROM mode omits the RAM's write port, instead taking its setup data from the JTAG programming interface during initial device configuration. Routing resources span two, three, and seven PFUs or PFFs in horizontal and vertical planes, and the clock-distribution network furnishes four primary and four secondary global clocks to complement the 12 internal routing signals that can also deliver clock signals.

The MachXO256 has single-ended input and output buffers with complementary outputs on 78-pin I/O banks, eight lines of which connect to a switch and nine more to LEDs on the evaluation board; the remaining lines appear on unpopulated header pads. To confirm the board's correct operation, the chip comes preprogrammed with a walking-LEDs display, which is also available from the company's Web site. The IDE's top level is Project Navigator, from which you open or create projects. Navigating to the \examples\fpga\MachXO subdirectory within the installation path reveals six subdirectories that contain a number of Verilog- and VHDL-format design files, such as 16-bit upcounters and downcounters. Invoking Project Navigator's Help opens a Web-browser window that provides an overview of available tutorials, user manuals, and sample projects. The *FPGA Schematic and HDL Design Tutorial*, which targets MachXO devices, introduces the IDE's mixed-mode design-entry capabilities, guiding you through top-level schematic and block-symbol creation, pin assignment, design-rule checking, and Verilog-model creation.

The product offers some neat features, such as the ability to assign multiple instances to a single symbol—in this case, a flip-flop—and the hierarchical navigator makes it easy to inspect the contents and connectivity of any object or net. All steps completed correctly until the last stage, when the design preplanner checks the pin and I/O assignments. At this point, two errors prevented the spreadsheet view of the device planner from opening. But these error messages pinpointed syntax errors within the source files, and double-clicking on each message opened a text editor with the cursor positioned at the error line, making repairs a breeze. From here, you can explore the other steps necessary to fit the design into silicon by following the flow that appears within the Processes for Current Source window, which keeps track of the design's current state. Finally, you can generate a programming file and physically test your work. Like all good software tools, the immediate appeal of this environment lies within its ease of use, and exploration will reward power users with facilities that lie beneath its surface. **EDN**

You can reach Contributing Technical Editor David Marsh at forncett@btinternet.com.

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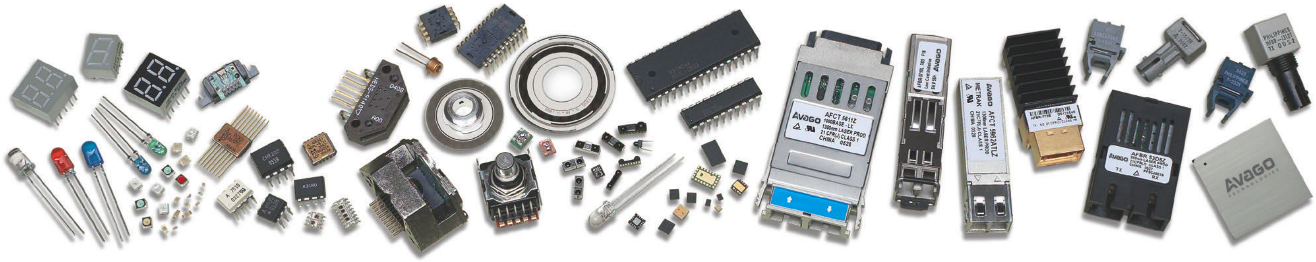

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BY SHYE SHAPIRA AND BORIS MISHORI • TOWER SEMICONDUCTOR LTD

Modeling gaps in state-of-the-art mixed-signal design

WITH THE EMERGENCE OF SOC DESIGNS, THE INDUSTRY HAS MOVED AWAY FROM THE IDM MODEL. TO ENSURE THAT YOUR DESIGNS WILL EMERGE FROM THE FOUNDRY AS YOUR SIMULATIONS PREDICT, YOU MUST EMPLOY STANDARDIZED AND ENHANCED COMPACT MODELS THAT ARE COMPATIBLE WITH ALL THE APPLICATIONS IN YOUR CIRCUIT.

The last two decades have seen the emergence of mixed-signal SOC (system-on-chip) design in which one IC integrates both analog and digital blocks. Meanwhile, the IC industry has overwhelmingly moved away from the IDM (independent-device-manufacturer) model in which companies design and manufacture ICs in-house, to the fabless model, in which systems companies design their own ICs but use third-party foundries to manufacture the devices.

As these two trends have matured, driven by Moore's Law (**Reference 1**), it has become difficult to ensure that the design you develop in your systems house will emerge as a robust chip from the foundry you are targeting. Designers can no longer rely on traditional compact models because they offer a limited description of electrical-device behavior. Due to the broad range of circuit applications implemented by fabless design houses, compact models may fail because they are often applied in ranges exceeding their scope of validity.

The addition of multiple new functions on a chip requires foundries to enhance compact models to address the effects of these additions and to adhere to a standard form that allows multiple companies to use these functions. IDMs have developed internal methods employing internal models and simulation platforms, each tailored to the IDM's specific applications, simulation tools, and design-flow methodologies. The new environment, on the other hand, requires you to devise a standard set of compact models that will have a broad range of coverage for all applications in the IDM, foundry, and fabless arena. Several professional organizations, such as the CMC (Compact Model Council, www.eigroup.org/cmc), are addressing these needs.

THE BSIM3 MODEL

In 1996, the CMC declared Version 3 of the BSIM3 (Berkeley short-channel-IGFET-model) MOSFET model from the University of California—Berkeley as the industry-standard MOSFET model (**Reference 2**). As a result of the standardization, all major simulation platforms use the model, allowing a relatively smooth transition from one simulator to another once you extract the model parameters on one platform. For five technology generations, this model has proved sufficient. However, scaling down dimensions of the transistors and reducing power-supply voltage reveal deficiencies in describing novel physical effects, as well as in the accuracy of operation. The developers of the BSIM3-model scheme based it on the Level 3 MOSFET-model approach, in which all voltages refer to source potential. The main parameter is the threshold voltage, which equals the gate-to-source-voltage difference at which an inversion layer emerges, forming the conducting channel. Different functions model different regions of operation. This approach causes discontinuity of the first derivatives, which is a nightmare for analog-system and high-frequency-system designers.

BSIM3 introduced smoothing functions between the subthreshold and strong-inversion regions that resulted in a single-function formulation, which removed discontinuity in current and voltage characteristics. Even though engineers have resolved the discontinuity problem, the model accuracy in the weak- and moderate-inversion regimes is limited because it is described by an empirical smoothing function. As a result, analog-system designers commonly use large transistors, which do not suffer from short-channel effects, and keep them in strong inversion and saturation.

This approach is successful in older technologies, in which high-supply-voltage (V_{DD}) values with respect to the thresh-

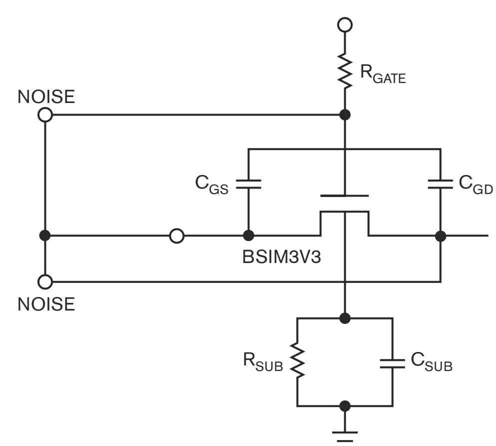
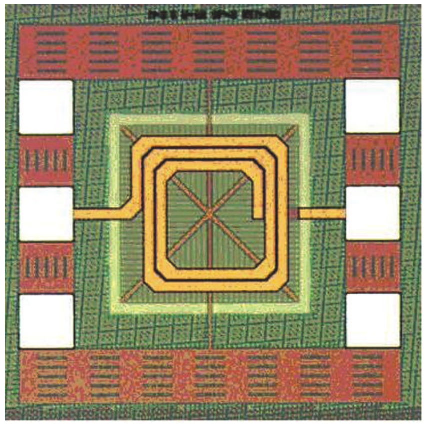


Figure 1 The MOSFET has a standardized BSIM3 Version 3 model. For RF applications, you must enhance the model with parasitic lumped elements, such as gate resistance, parasitic capacitance, and noise sources, which you can implement in subcircuits. When not standardized, these constructions may lead to errors in construction or when translating between simulators.

old voltage (V_{TH}) provide designers with a lot of margin for the voltage range of operation. For advanced technologies, however, the V_{DD}-to-V_{TH} gap is significantly smaller, and designers must operate MOSFETs in poorly modeled moderate- and weak-inversion regimes. They also must use small MOSFETs with short-channel effects to comply with cost-reduction constraints. These requirements do not allow designers to use a simple description of the device behavior, such as the "square law": $I_{DS}=(V_{GS}-V_{TH})^2\times(uWC_{OX})/(2L)$, where I_{DS} is the drain-to-source current, V_{GS} is the gate-to-source voltage, u is the carrier mobility, W is the channel width, L is the channel length, and C_{OX} is the gate capacitance. Consequently, designers need a highly accurate model of moderate- and weak-inversion modes. Current V_{TH} models provide poor coverage for such issues as non-quasistatic behavior, high-frequency-noise modeling, and the accurate description of the large dynamic range of currents for circuits such as R2R, which are ladders of current mirrors giving current outputs at given fractions of an input current (**Reference 3**).



This photo shows a test structure for RF modeling of an inductor. Many passive devices, such as inductors and resistors, require complex modeling. Currently, you achieve this modeling using subcircuits. However, the modeling is not standardized, and its use may lead to errors when you construct the subcircuits or when you translate them from one simulator to another (courtesy Sharon Levin, Tower Semiconductor).

NEXT-GENERATION STANDARDIZED MOSFET

Surface-potential-based models, which describe the MOSFET behavior as a function of the electrostatic potential in the channel, preserve physical behavior and correctly reproduce current and voltage characteristics and their derivatives. The better preservation of derivatives also guarantees that such models better serve RF applications, which strongly depend on derivatives of currents.

As a result of the shortcomings of current V_{TH}-based models for advanced technologies and applications, the CMC two years ago initiated next-generation-MOSFET-model standardization. During the process, the CMC decided to base the model on surface potential. Recently, the CMC reached a milestone when it selected Pennsylvania State University's (www.psu.edu) and Philips' (www.philips.com) PSP (Penn State-Philips) model for standardization (**Reference 4**). The model competed with Hiroshima University's (www.hiroshima-u.ac.jp) HiSIM (Hiroshima University STARC IGFET Model) compact MOSFET model. Initially, the CMC was considering the University of California—Berkeley's BSIM5 and the EKV (Enz-Krummenacher-Vittoz) MOS model. The selection process included comparison with 90-nm-MOS-data computational efficiency and robustness, along with a host of physical signatures that the CMC expected the model to exhibit. Currently, standardization work for the PSP model is ongoing, and most vendors' simulation platforms already include it.

NON-MOSFET-STANDARDIZATION GAPS

Resistor modeling shows the most striking examples of the lack of some essential features and standardization. Standards makers gave the resistor models lower priority because resistor-model structures seem simpler than those of MOSFETs. Although several models are available in standard simulators, many fab offerings include a subcircuit containing several segments of a basic resistor and parasitics. You must exercise care when using the redrawn simulator model's topology and when translating a model between simulators to ascertain that they are identical and that no errors arise in the assignment of area or parasitic-diode polarity. This scenario contrasts with the more complex MOSFET model, which you compile into a simulator and, aside from slight differences, performs identically in different simulators once you extract the model parameters.

The use of the models in the PDK (process-design kit) is more complex than that for MOS models even in mundane aspects. For example, the PDK needs to provide a special instance name when using a subcircuit model, which is necessary for using the segmented resistor subcircuit, in some simulators. Foundries currently offer basic resistor models that display voltage and temperature coefficients describing resistance variability. The voltage coefficients give some description of the resistor variation with terminal voltage, but they may be misleading to inexperienced designers because their validity applies only to the geometries for which the foundry characterized them. The electric field most directly affects transport in bulk materials, such as diffusion resistors. To demonstrate the limitations in modeling using voltage coefficients, consider, for example, a resistor with a voltage dependence of $R=R0(1+AV)$, where V is the voltage between the resistor's terminals, R0 is the resistance with low-voltage bias, and A is a linear-voltage coefficient. With resistors of sufficiently low voltage, you can ignore higher order voltage coefficients. If you employ Ohm's Law and consider the resistor as two resistive sections in series, each experiencing a voltage drop of V/2, you get $R=2\times R0/2(1+AV/2)=R0(1+A/2\times V)$. Hence, you arrive at a new voltage coefficient that depends on how many sections the resistor has.

On the other hand, to describe the resistance as dependent on electric field, you could use the equation $E=V/L$, where E is the electric field, V is the voltage, and L is the resistor length. In this case, $R=R0(1+A\times E)=R0(1+A\times V/L)$, and, for a two-section resistor, each section would have half the voltage and half the length and hence still experience the same electric field: $R=2\times R0/2[1+A\times(V/2)/(L/2)]=R0(1+A\times V/L)$. In practical terms, if you model a resistor's voltage coefficients, the model is valid only for the geometry for which the foundry characterized it. With positive-voltage coefficients, shorter devices exhibit larger voltage dependence due to the stronger electric fields. Fabs recommend using large area resistors for accuracy; these resistors also work well for correcting width and mismatch variations. They correct the modeling gap by complementing the volt-

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The PFC FrontEnd is an extremely low profile, 1 RU enclosed chassis mount AC front end that may be used with any 300 V VI-200 / VI-J00 or 375 V Vicor Maxi, Mini, Micro Series modules, VIPAC Arrays, or other modules to create a complete, high density AC-DC power supply. Accepting universal input voltages of 85 Vac to 264 Vac, and 100 to 380 Vdc, the PFC FrontEnd can deliver up to 2,200 W @ 230 Vac from 4 non-isolated outputs (additional using "Y" adapters). With an extremely compact package size of 1.72″ H (43,6 mm) x 6.4″ W (162,6 mm) x 7″ L (177,8 mm), the PFC FrontEnd can provide >28 W/in^3.

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age-coefficient data with characterization data for shorter devices. The basic resistor models also fail to cover the resistor-body effect, which is the variation of the resistance with substrate voltage.

The CMC recently began standardizing the resistor model to an electric-field-based model. It is currently adopting the two-terminal resistor model, which now includes temperature- and electric-field-dependent coefficients, self-heating, and 1/f noise. The CMC is also considering standardization for other components, including accumulation capacitors, three-terminal resistors, and laterally diffused MOSFETs.

Although the CMC has addressed models' features and robustness, it has not addressed their viability as products in standard industrial use. For example, designers want to know how easy it is to create a netlist with a compact model or how to use the model to describe process variations. Typically, process variations are modeled as "corner cases," depicting extreme envelopes of device performance. The CMC has developed and standardized models to describe the behavior of a typical device. The method of defining the corners is the task of the modeling group, rather than the standards makers. In more accurate modeling procedures, such as statistical modeling, designers simulate many instances of the same model to describe the variation in electrical behavior that occurs because of process variations. Although every modeling group develops its own version of how to produce corner cases or statistical-model cases, they invest little attention in choosing model parameters that would allow easy production of corner cases.

Another example of lack of standardization is the mismatch modeling describing the variations between identical devices on a chip. Current models cover neither mismatch modeling nor statistical modeling, leaving them to modeling groups to construct. Because the standardization is absent, the translation between simulators is prone to the same problems as those of segmented-resistor models.

The FSA (Fabless Semiconductor Association) has begun to address some of these model-standardization procedures. The compact models are part of the constantly evolving standards ecosystem, which includes the foundries' modeling engineers, the vendors' IC designers, intellectual-property vendors, EDA companies, and PDK developers. The FSA recognized the complexity of this situation and founded working groups such as the MSRF (Mixed-Signal/Radio-Frequency) PDK Working Group, MSRF Model Working Group, and MSRF IP (Intellectual Property) Working Group. These groups' main goals are to define requirements in MSRF-design services, libraries, modeling, IP, wafer processing, assembly, and test; to standardize the information-distribution format; and to define quality criteria. As a result of this activity, major foundries have prepared and adopted PDK and MSRF Spice-model check lists. These documents include informa-


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tion about compact models, design-rule files, and parameterized cell generators. Fabless companies can use this information to easily compare various foundries' model-quality and design-environment kits to decide on second-sourcing or design-transfer arrangements.

Although both the FSA and the CMC have greatly advanced the standardization of models, gaps still exist. In the coming years, these organizations and tool vendors face the challenge of standardizing these simulation platforms to satisfy the need for compact models for the increasing number and variety of analog-circuit applications. **EDN**

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AUTHORS' BIOGRAPHIES

Shye Shapira, PhD, is director of research and development in the RF and mixed-signal product line at Tower Semiconductor (Migdal Haemek, Israel). Previously, he worked as a research associate at the Cavendish Lab of the University of Cambridge (England) and was a member of the technical staff at Lucent Technologies and Agere Systems. He has bachelor's, master's, and doctorate degrees in physics from Physics Department Technion IIT (Haifa, Israel). His personal interests include device physics and novel device-physics effects as enablers to RF- and power-circuit design. You can reach him at shyesh@towersemi.com.

Boris Mishori, PhD, is the head of Spice modeling and interconnect parasitic extraction at Tower Semiconductor (Migdal Haemek, Israel), where he has worked since 2001. Previously, he worked as a research associate at the City University of New York. He has bachelor's and master's degrees in science from the Minsk Radio Engineering Institute (Belarus) and a doctorate from Tel Aviv University (Israel). His personal interests include device physics and compact models of MOSFET-technology devices for analog and RF applications. You can reach him at borismi@towersemi.com.

Isolated and Non-Isolated High Power, High Voltage DC/DC Controllers

High Performance Analog Solutions from Linear Technology

A very familiar and simple approach to designing an isolated DC/DC converter is the flyback topology. The conversion of an input voltage to an isolated output and the transfer of signals between the high voltage and low voltage planes can be accomplished with the use of transformers and optoisolators. Linear Technology has introduced a new family of flyback converters that are simple and require no optoisolator. Although the flyback converter is used in both non-isolated and isolated power supplies, an isolated design is important when protecting the load (i.e. 1.5V FPGAs) from a high input voltage (72V) by eliminating a direct electrical path from the input to the load ("isolating" the load from the input supply). Isolated flyback DC/DC power supplies are typically found in telecom wireless networks, RFID base stations, Power-Over-Ethernet (PoE) systems and medical instruments, among others.

The flyback topology offers simple isolated DC/DC conversion; however, it is most commonly used in the 30W-50W output power range. This is mainly due to the limitation of the output diode with its inherent high power losses potentially causing ther-

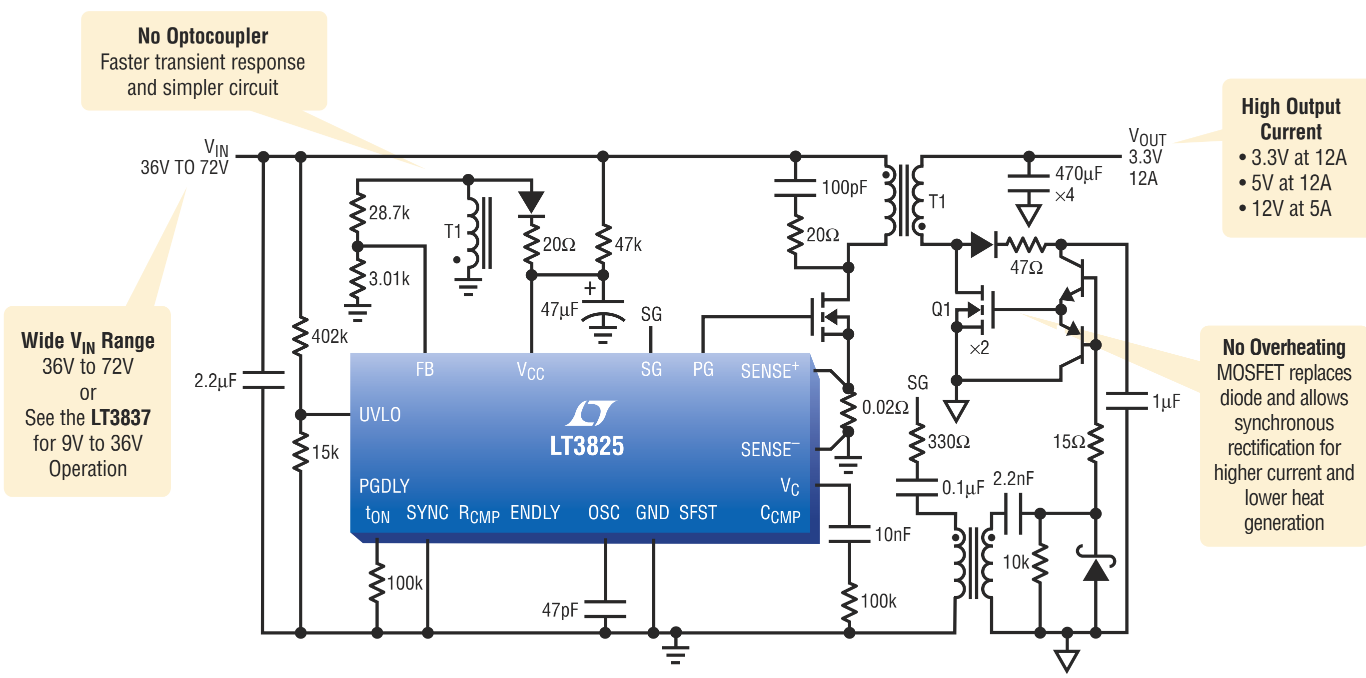

Figure 1. The LT®3825 (or LT3837) Incorporates Synchronous Drive Circuitry and No Optocoupler Design for Delivery of High Current at High Efficiency with Fast Transient Response

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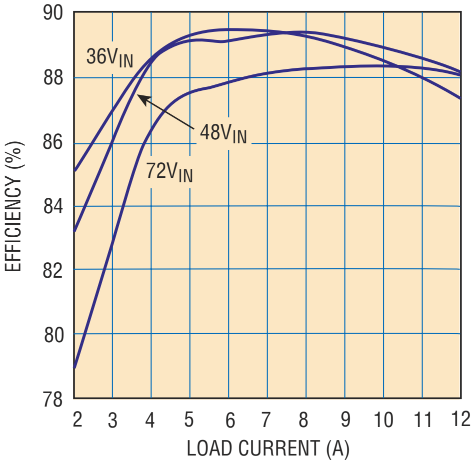

Figure 2. High Efficiency vs. Load Current for Circuit in Figure 1

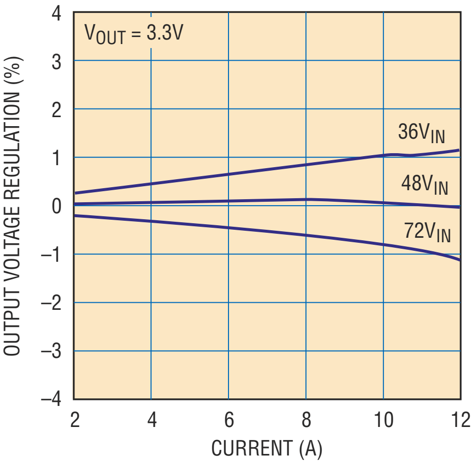

Figure 3. Precision Output Regulation Is Within ±1.3% for Current in Figure 1

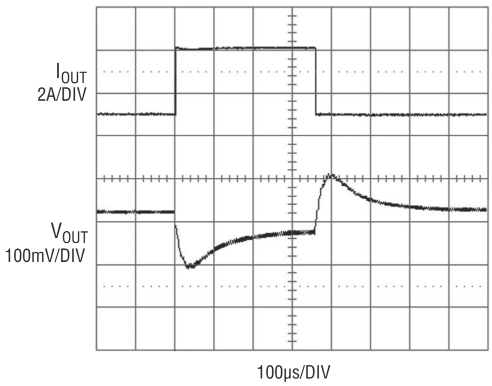

Figure 4. No Optocoupler Design Allows the LT3825 and LT3837 to Deliver Fast Transient Response

mal problems. Above this power level or load current, designers usually adopt other topologies to prevent excess heat dissipation in the output diode, which can increase the complexity and cost of the design. Often designers push their flyback circuits close to or beyond the safe operating temperature to achieve higher output currents. This jeopardizes a power supply's reliability especially when the system is enclosed and has limited air flow for cooling.

An isolated synchronous flyback controller bridges the gap between the standard low current flyback and the higher current but more complex topologies. It allows a flyback topology to quadruple the load current capability while operating safely at lower temperatures.

12A Flyback Power Supplies without overheating

The LT3837 and LT3825 are flyback controllers that incorporate the control circuitry for synchronous operation. In addition to synchronous operation for higher load current delivery at higher efficiency (Figure 2), this family offers a simpler solution by eliminating the need for an optocoupler and its driver circuitry while also improving performance. This not only reduces the circuit footprint but also reduces design complexity. The LT3825 targets the telecom (36V-72V) market where the input has a 2:1 ratio (low to high end). The LT3837 (Figure 5) is optimized for lower input voltage operation of 9V to 36V or 4:1 ratio (Table 1). The internal circuitry for each part has to be designed so that functions such as UVLO, bias and gate drive perform optimally for both input ranges.

A standard non-synchronous flyback circuit satisfies load current requirements of approximately 3A. Above 3A, the output diode may become too hot. It is because of this rise in temperature that non-synchronous flyback circuits are limited in output load delivery. The LT3825 and LT3837's synchronous drive eliminates this problem by replacing the Schottky diode with a MOSFET. A MOSFET has much lower voltage drop when conducting

Table 1. LT3837/LT3825 Synchronous Flyback Controllers

	LT3837	LT3825
Topology	Synchronous Flyback	
Output Power	≤60W	
Synchronous Rectifier Driver	**Yes**	
Optoisolator and Reference	**Not required**	
Input Range	9V to 36V	36V to 72V
Package	16-Lead TSSOP exposed pad (LT3825 and LT3837 are pin compatible)	

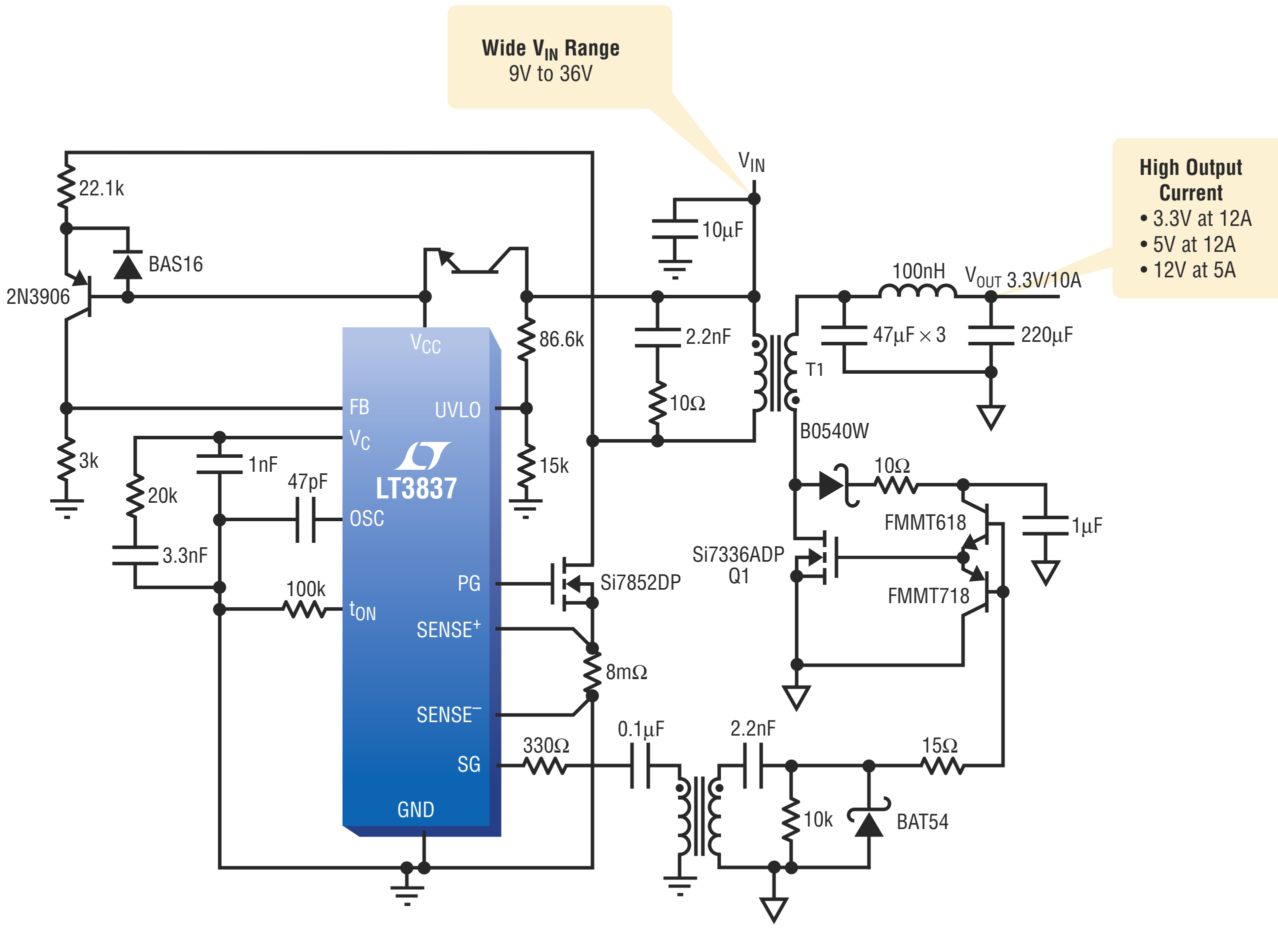

Figure 5. The LT3837 Synchronous Flyback Controller Is Optimized for 9V to 36V Input Supplies for Industrial and Instrumentation Applications

current than a diode and therefore produces less heat. An LT3825 circuit can deliver 12A to a 3.3V load (Figures 1 and 2).

No Optocoupler, Fast Transient Response

Instead of using a part's intensive secondary-side voltage reference, error amplifier and optocoupler, the primary bias winding on the flyback transformer (T1) is used. Feedback circuitry inside both the LT3825 and the LT3837 reads the reflected output voltage information on this winding during the flyback pulse. This voltage is then compared to a precision internal reference and an error signal is obtained. The error signal is used to modulate the on-time of Q1 in such a way as to regulate the output voltage. An important benefit of this technique is that output voltage information arrives at the controller instantly after the switching cycle is terminated, resulting in fast transient response to changes in load (Figure 4). In a conventional optocoupler-based

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design, a propagation delay of several microseconds occur in the optocoupler alone, severely limiting the converter's transient response.

60V, 100% Duty Cycle 40µA I_Q Step-Down Controller

The LT®C3824 is a 4V to 60V input range, 100% duty cycle, low I_Q, adjustable switching frequency 100kHz to 600kHz, DC/DC current mode controller. This controller is ideal for automotive requirements where the 4V low end input works during cold cranking and the 60V high-end input works during inductive load dumps, without the need of external clamping circuits. The 40µA quiescent current minimizes the drain on the car battery when in standby mode.

The LTC3824 offers step-down solutions for applications that cover a broad range of inputs, from battery-powered instruments to automotive requirements, where the $60V_{IN}$ maximum rating allows much more V_{IN} margin than most other controllers.

The benefit of 100% duty cycle is to have the lowest possible dropout voltage to extend battery life, allowing V_{OUT} to equal or be close to V_{IN}. The LTC3824 drives an external P-channel MOSFET and maintains high efficiency at light loads with its Burst Mode® operation and 40µA no load quiescent current. The current mode operation provides fast line and load transient response as well as cycle-by-cycle overcurrent protection. Additional features include short-circuit protection, adjustable soft-start, overvoltage protection and undervoltage lockout. For noise-sensitive applications, the LTC3824 can be easily synchronized to an external clock from 100kHz to 600kHz. In addition, the output voltage can be adjusted over a wide range from 0.8V to V_{IN}. The LTC3824 is offered in a 10-pin thermally enhanced MSOP package.

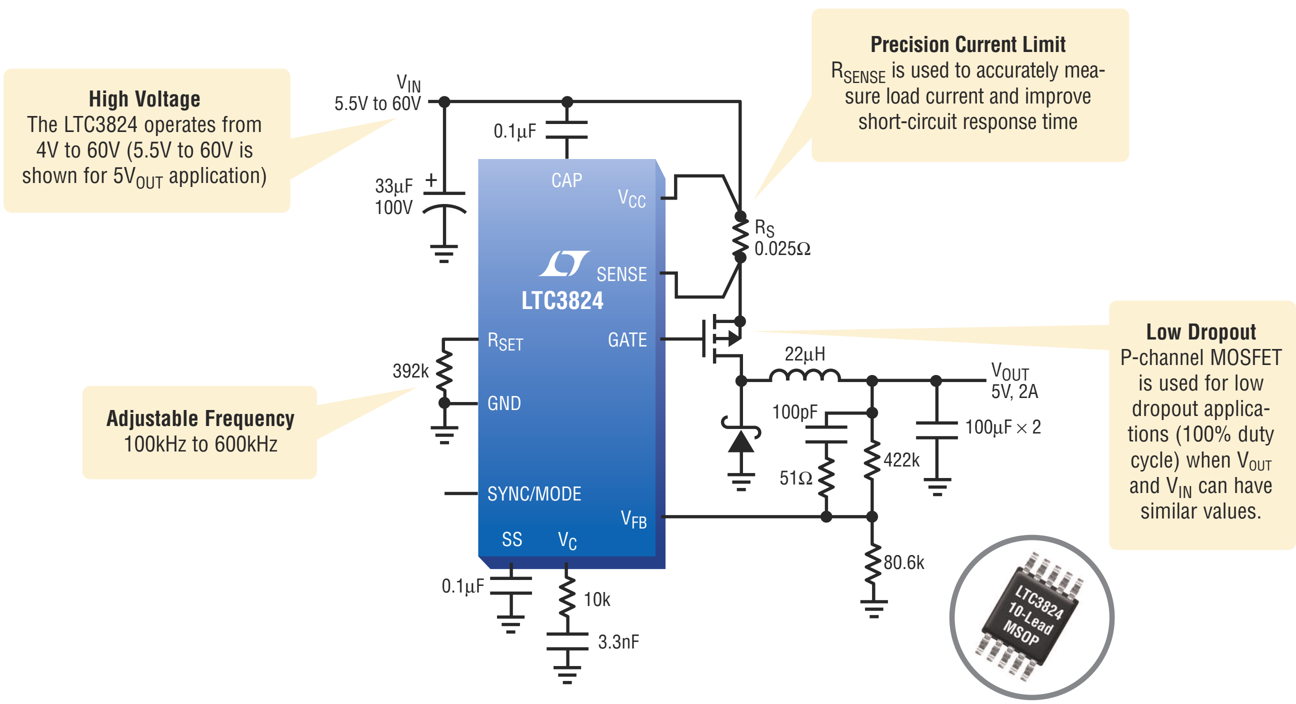

Figure 6. Easy-to-Use Non-Isolated High Voltage Buck Controller

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BY MARK HOLDAWAY • XIGNAL TECHNOLOGIES AG

Designing antialias filters for ADCs

CONTINUOUS-TIME ADCs CAN BENEFIT SIGNAL-CHAIN DESIGN. AN OVERVIEW OF DISCRETE- AND CONTINUOUS-TIME SYSTEMS DETAILS THE DIFFERENCES.

Nyquist-sampling theory lies at the heart of today's digital-communications systems. It requires that data-conversion systems include antialiasing input filters. Designers need to understand the requirements for antialiasing filters and examine the consequences of filter application. They must also consider the benefits of a new class of ADC that uses a low-power, high-speed, continuous-time-sampling method. These devices claim the ability to achieve a first Nyquist-zone-sampling capability without the aid of external filters.

You can reconstruct a time-continuous signal from discrete-time-sampled data if the original sampling rate is twice that of the highest frequency component in the sampled signal. The Nyquist-sampling theory states that data clocked with a sample rate of f_S (sampling frequency) samples/sec can effectively represent a signal of bandwidth as high as $0.5\times f_S$ Hz. The Nyquist theory places demands on the sampling function, time, and amplitude precision. Sampling signals with signal content greater than a $0.5\times f_S$-Hz bandwidth cause aliasing, a nonlinear process that results in frequency shifting. Signal content at frequencies greater than $0.5\times f_S$ Hz folds around $0.5\times f_S$ Hz—the Nyquist frequency—and alias back into the baseband. This aliasing creates a serious problem: Once you sample the signal, you have no way of determining which resulting signal components originate from the desired signal band and which ones are aliased errors. **Figure 1** shows two alias signals, A′, a single tone, and B′, a spectrum, each folding down into the first Nyquist zone. Note that A′ originates in Nyquist Zone 4, and B′ is from Zone 3. Also note that, in a communications application, this folding may allow interference signals to completely obscure information-bearing Signal A.

You should bandlimit a signal for digitization to eliminate any signal power beyond the frequency range of interest. The design of a suitable antialiasing-filter network may seem fairly trivial; however, as ADC linearity and performance improve, these filters become a significant part of the total system design.

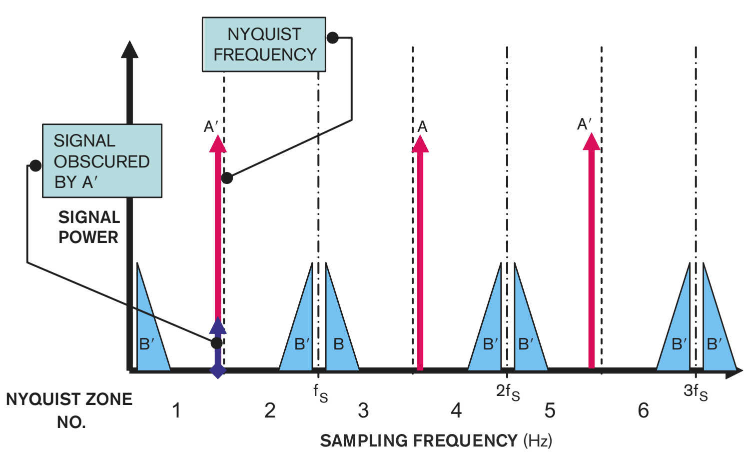

Figure 1 Alias signals A′, a single tone, and B′, a spectrum, can reside in any Nyquist zone if no antialias filter exists in a sampled system, but you can find both in Zone 1, where A′ now obscures an information-bearing tone. A originates in Nyquist Zone 4, and B is from Zone 3.

IDEAL AND PRACTICAL FILTERS

Ideal baseband, lowpass antialiasing filters should have a steep transition band, excellent gain flatness, and low distortion in the passband—difficult goals to achieve. Furthermore, the stopband attenuation should be enough to reduce any residual out-of-band signal power to a level invisible to the ADC. You achieve this performance by employing stopband attenuation in excess of the dynamic range of the ADC (**Figure 2**). Assume that the stopband extends to infinity. Applications encountering high noise levels, especially those with high levels of interference occurring close to the edge of the first Nyquist zone, require filters with aggressive falloff. You achieve this performance using high-order filters that typically exhibit poor phase performance and result in dispersion or large group delay. In antialiasing filters, filtering takes place before the time-sampling point, or quantizer; these filters consequently require the use of an analog filter. This requirement is unfortunate because you can more easily and cost-effectively implement aggressive filters in the digital domain. High-order analog filters provide low harmonic distortion and gain flatness to in-band signals. However, the design of these filters is complex because they are too sensitive to gain matching to be practical at more than a few orders of attenuation magnitude. Furthermore, any passband harmonic distortion the filter introduces also produces undesirable signals in the output spectrum of the ADC. Insertion loss might also be important when using passive filters, which increase system noise.

An ideal antialiasing filter features 0-dB unity gain in the passband with little or no gain variation and a level of alias attenuation that matches the theoretical dynamic range of the data-conversion system in use. You derive a first approximation of this value from the theoretical SNR (signal-to-noise ratio) for an N-bit ADC: SNR=6.02×N+1.76 dB. For a 14-bit ADC, this approximation requires 80- to 86-dB attenuation with an ideal SNR of approximately 86 dB.

A number of standardized filter-transfer functions, including Bessel, Butterworth, Chebyshev, and elliptic, exist. Each has specific characteristics in the passband, transition band, and stopband. Selecting the appropriate topology depends on the most critical performance aspects of a design. Butterworth filters have the flattest passband region and minimal group delays. Chebyshev filters have steeper roll-offs but more passband ripple. Elliptic filters feature the steepest roll-off (**Figure 3**). The **figure** does not show a Bessel filter, which has a more gradual roll-off but has the key advantage of a linear, or constant, phase response. A number of public-domain tools exist to help developers in the design of a suitable antialiasing filter.

A consequence of using an antialiasing filter is the limit on available alias-free bandwidth when you use it in a traditional ADC. At first glance, the Nyquist theorem seems to promise a lot. Consider an ADC that samples at 40M samples/sec at a clock frequency of 40 MHz. It theoretically promises a 20-MHz signal bandwidth. However, aliasing with practical filter design means that the free bandwidth is considerably less than this amount. A 14-bit converter can resolve to one part in 2^{14}—that is, one part in 16,384. To bury any alias component in the ADC's noise floor requires attenuation to be less than ±0.5 LSB. That amount equates to 90-dB attenuation—that is, ±0.5 LSB=one part in 32,768=90.3 dB. In practical terms, however, this level of attenuation need exceed only the measured SNR of a 14-bit ADC. A more realistic level in the filter design is an attenuation of 80 dB.

Figure 3 shows several possible filter topologies, including two Butterworth-transfer functions—those of four- and eight-pole systems—both compared with an ideal Nyquist filter. Note that, by convention, the cutoff frequency is the point at which the filter produces 3 dB of attenuation. The horizontal axis shows the normalized input frequency as a ratio of the absolute frequency to the cutoff frequency. Note that the four-pole curve does not drop to 80 dB until the input frequency has risen to 10 times the cutoff frequency. So, if this ADC were to sample a 5-MHz signal, then this system would still see frequencies all the way out to 50 MHz. To fully sample the 5-MHz bandwidth and eliminate aliasing, the correct sample frequency using this filter would need to be 100 MHz. The range of 5 to 50 MHz becomes a guardband against alias errors. An obvious option is to look for higher performance filters. Consider an aggressive, eight-pole filter. Inspection shows that the 80-dB-attenuation point occurs at a frequency that is 3.2 times the cutoff frequency, or 16 MHz, a significantly reduced alias guardband. Alias-free sampling requires considerably more system bandwidth to handle the alias-guardband needs of an application. It is also important to note the cost trade-offs you must weigh when considering the severity of the antialiasing filter and the performance level of the ADC.

To ease antialiasing-filter design, pipeline ADCs—often confusingly referred to as Nyquist converters—have been offering increased sample rates and input bandwidths. Oversampling a signal at twice the Nyquist rate evenly spreads the ADC's quantization-noise power into a two-

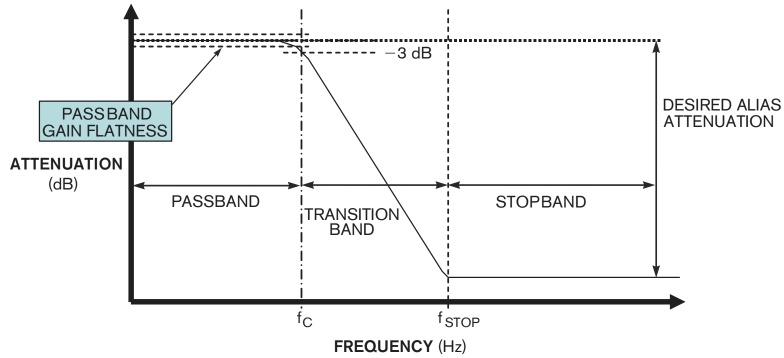

Figure 2 Ideal lowpass antialiasing filters should have a steep transition band, excellent gain flatness, and low distortion in the passband.

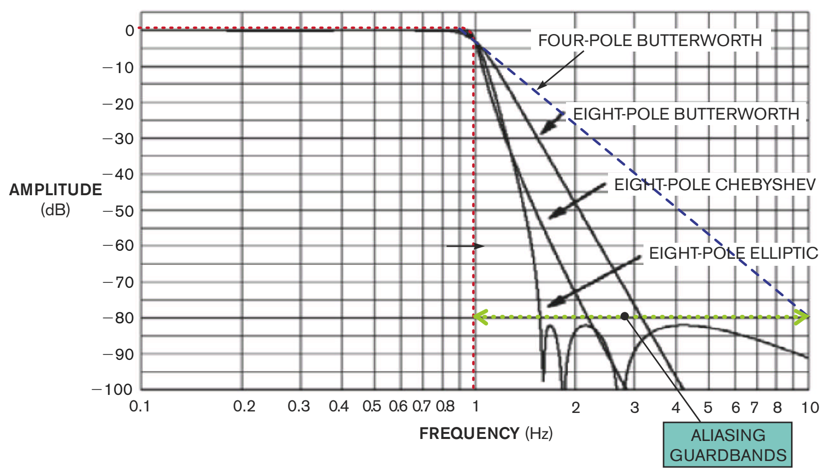

Figure 3 Possible antialias-filter designs illustrate the different transition-band characteristics of example filter systems.

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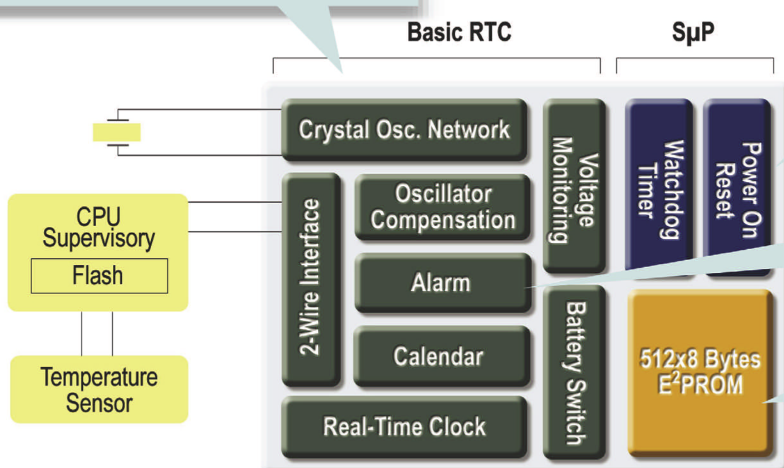

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ISL12026	512 X 8	2	N	N	$\overline{IRQ}/F_{OUT}$		5 Sel. (2.63V to 4.64V)	8-Ld SO/TSSOP
ISL12027	512 X 8	2	Y	Y	RESET		5 Sel. (2.63V to 4.64V)	8-Ld SO/TSSOP
ISL12028	512 X 8	2	Y	Y	$\overline{IRQ}/F_{OUT}$		5 Sel. (2.63V to 4.64V)	14-Ld SO/TSSOP
ISL12029	512 X 8	2	Y	Y	$\overline{IRQ}/F_{OUT}$		5 Sel. (2.63V to 4.64V)	14-Ld SO/TSSOP

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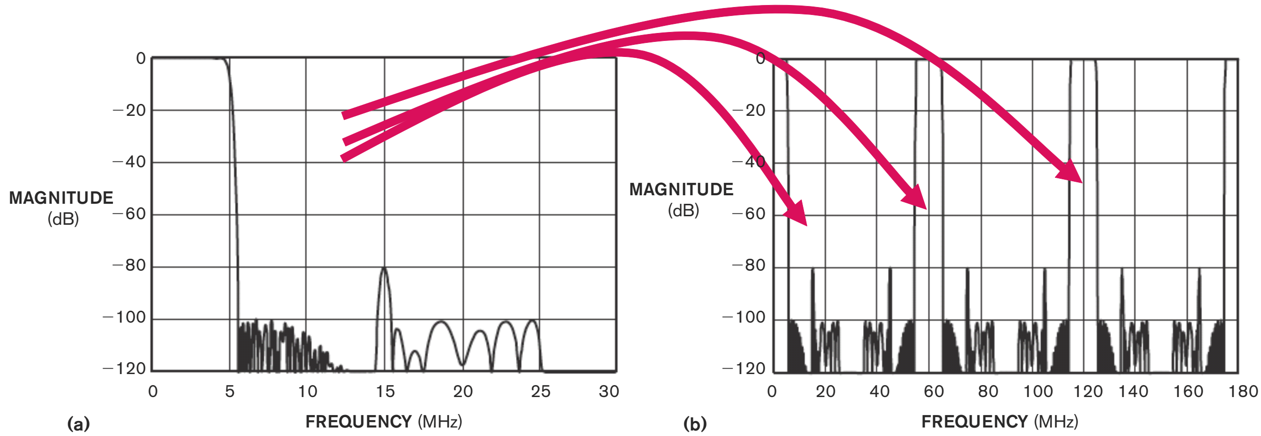

Figure 4 Discrete time sampling produces a lowpass signal-transfer function in a discrete time delta-sigma ADC (a). The graph in (a) appears to show alias protection; however, the transfer function of (a) is wrapped around integer multiples of the sampling frequency, as the expanded plot (b) shows. Aliasing gaps appear centered on 60, 120, and 180 MHz in this case.

times-wider frequency band. Applying decimation to subsample the resultant output samples yields a 3-dB/octave conversion gain. This technique is useful for deployment in delta-sigma converters because it not only produces dynamic-range improvements, but also reduces the pressure on the antialiasing filter by relaxing filter roll-off. Lower order antialiasing filters are easier to match across multiple channels than higher order ones. Oversampling techniques reduce the demands on the filter networks, but higher-sample-rate ADCs and faster digital processing use more power and increase cost.

You must also consider the phase response of the antialiasing filters. A filtered signal should not see any significant phase alteration. This alteration becomes even worse if phase varies according to input frequency. You normally measure phase variation in a filter in terms of group delay—that is, the derivative of phase with respect to frequency. For a nonconstant group delay, a signal spreads out in time, causing poor impulse response. Dispersion may be an additional worry for system performance. This factor is important in the design of

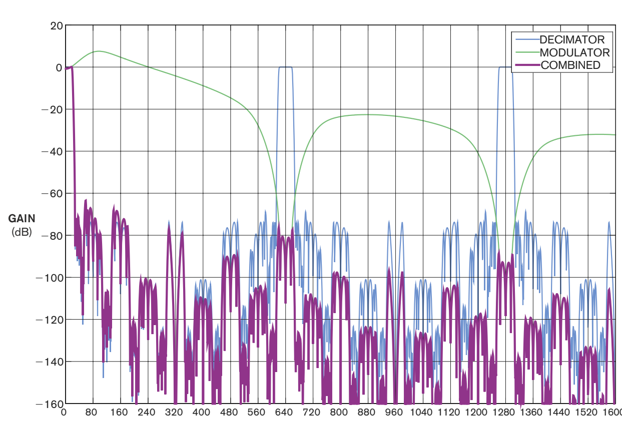

Figure 5 An aliasing-mitigation system ensures the analog-loop filter provides maximum stopband attenuation at the oversampling frequency of the modulator.

ultrasound systems in which the received-signal phase carries reflection information.

DELTA-SIGMA CONVERTERS

Delta-sigma techniques place lower demands on antialiasing filters. Delta-sigma converters exploit oversampling. In the past, designers improved dynamic range by using high oversampling rates and a simple low-resolution quantizer. However, simple oversampling produces minimal conversion-gain improvements. Applying feedback provides a faster route to conversion-gain improvements.

Delta-sigma modulators apply feedback to shape the quantization noise in the frequency domain by pushing most noise power into frequencies beyond the signal band of interest. Filtering can reduce the noise power in this band. Employing oversampled systems, which provide free frequency space beyond the signal band of interest, accomplishes this goal. Conventional Nyquist converters achieve a 3-dB/octave conversion gain through 2× oversampling. Delta-sigma converters more efficiently build conversion gain, which the order of the applied feedback loop determines. First-, second-, or third-order loops can provide 9-, 15-, or 21-dB/octave conversion gain, respectively.

Most delta-sigma-converter implementations are discrete-time systems in which designers build the loop-filter components from simple switched-capacitor filters. The signal-transfer function of a delta-sigma modulator is an important factor in such a design. Signal-transfer performance looks promising in traditional discrete-time systems. Digital-decimation filters define the effective passband and provide a sharp transition band. Unfortunately, switched-capacitor-filter networks, which define the input bandwidth, add a discrete-sampling effect to the modulator structure. This discrete sampling causes a lowpass signal-transfer function (**Figure 4a**). Although this function seems acceptable, a closer inspection of a wideband-frequency plot reveals a problem: The passband of the digital filter wraps around integer multiples of the sample frequency at 60, 120, and 180 MHz (**Figure 4b**). No alias attenuation whatsoever exists at these points, and this characteristic extends to infinity. Preventing high-level, out-of-band noise at multiples

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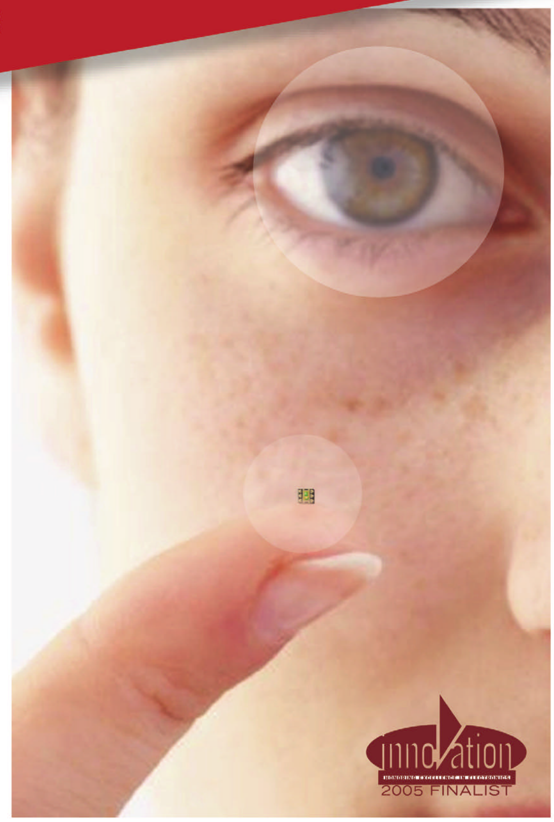

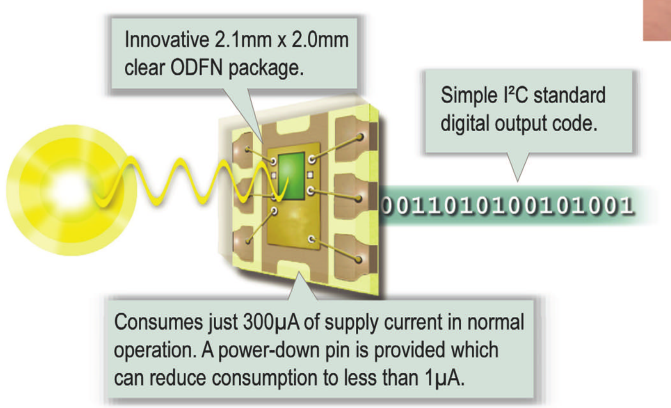

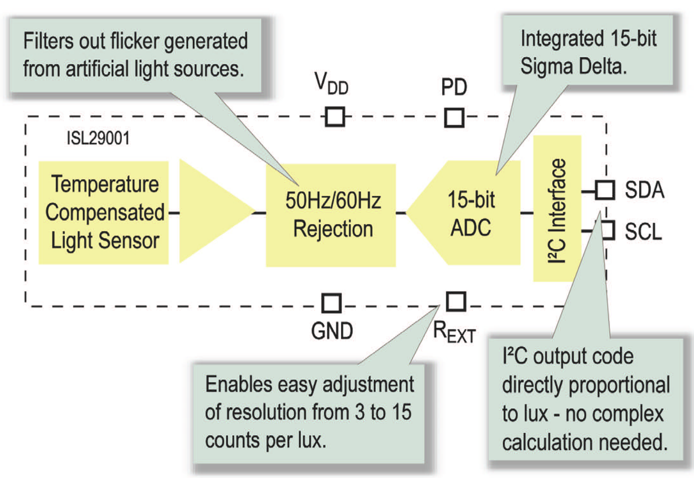

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of the oversample rate is a challenge and a downside of such designs.

CONTINUOUS TIME

In a continuous-time modulator, you implement noise shaping using conventional analog active filters. The benefit of the continuous-time approach is that you can design the loop filter to handle alias filtering of the input signal. Tailoring this filter system for a specific product, the maximum-loop-filter attenuation coincides with the minimum attenuation that the decimation filter offers. An aliasing-mitigation system ensures that the analog-loop filter provides maximum stopband attenuation at the oversampling frequency of the modulator (**Figure 5**, green line). This attenuation ensures that no noise power beyond the oversampling frequency can enter the first Nyquist zone. The back-end digital filter provides a sharp stopband attenuation, limiting the maximum effective input bandwidth of the ADC (blue line). Through this arrangement, the maximum analog-loop-filter attenuation always coincides with the folded-digital-filter minimum to maintain a high level of wideband attenuation. The maximum attenuation of the analog-loop filter coincides with the alias passband of the digital filter. The purple line shows the composite transfer function.

The specific implementation of a given delta-sigma topology determines the performance of the antialias system. For example, the 14-bit-resolution, 20M- to 40M-sample/sec Xignal (www.xignal.com) XT11400 ADC achieves 76-dB SNR and provides a 20-MHz analog-input bandwidth. The passband gain flatness is ±0.002 dB, the transition band is approximately 2.5 MHz wide, and the unit achieves alias attenuation of 80 dB beyond 22.5 MHz, all without any external filtering. A digital allpass-filter stage, which reduces dispersion to 0.3 samples, minimizes group delay. Such approaches have benefits in reducing design complexity, especially in multiple-channel designs in which cross-channel filter matching is a major issue.

In summary, delta-sigma modulators use oversampling to help simplify anti-aliasing-filter design. For discrete-time systems, you must use caution in designing antialiasing filters because of the potential occurrence of high-frequency noise, which can couple and fold directly into the baseband. A continuous-time alternative can eliminate the need for all external antialiasing filters. The maximum attenuation of the analog-loop filter aims successfully to intercept the passband frequency of the digital-decimation filter at the oversampling frequency. EDN

AUTHOR'S BIOGRAPHY

Mark Holdaway is product-marketing director at Xignal Technologies AG (Unterhaching, Germany). He holds a bachelor's degree in electronics engineering from the University of Salford (England). His interests include cycling, skiing, gardening, reading, and writing. You can reach him at mark.holdaway@xignal.com.

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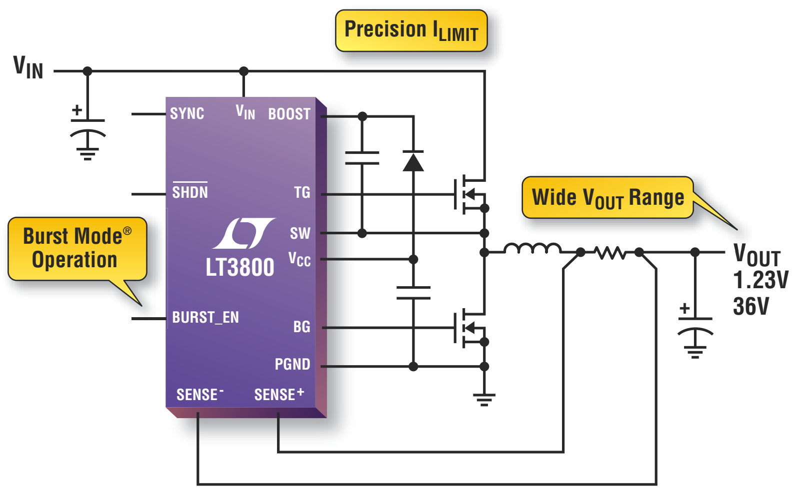

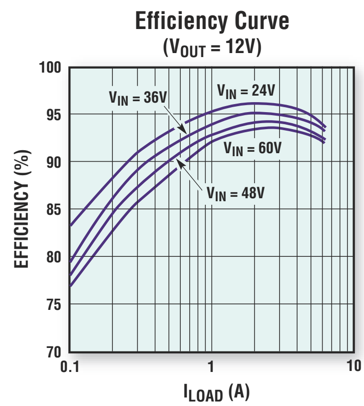

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Switchmode Controllers							
LT®3844	10	4 to 60	1.23V to 36V	120	100 to 600	100 to 500	Adjustable Frequency
LT3724				80	-	200	Fixed 200kHz Operation
LTC®3824			0.8V to V_{IN}	40	200 to 600	200 to 600	100% Duty Cycle, Low Dropout
LT3800	20	4 to 60	1.23V to 36V	80	-	200	Synchronous Drivers
LT3845				120	100 to 600	100 to 500	
Switchmode Monolithics							
LT3437	0.4	3.3 to 80	1.25 to 0.9xV_{IN}	100	240 to 700	200	Ultrawide V_{IN}
LT1976	1.3	3.3 to 60	1.2 to 0.9xV_{IN}	100	230 to 700		
LT3434	2.5	3.3 to 60	1.25 to 0.9xV_{IN}	100	230 to 700		

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A Compact Dual Step-Down Converter with V_{OUT} Tracking and Sequencing – Design Note 403

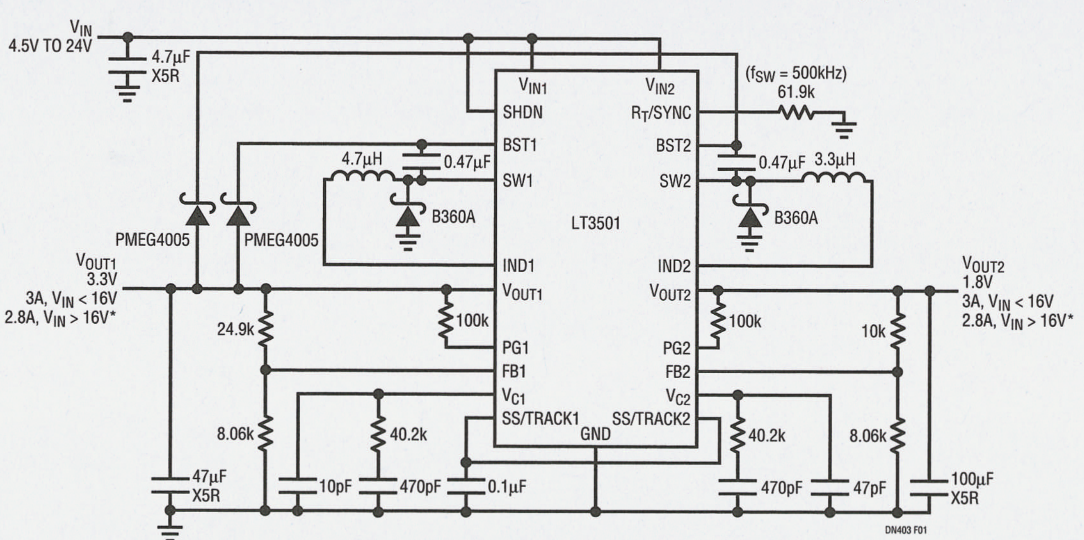
Tiger Zhou and David Canny

Introduction

Typical industrial and automotive applications require multiple high current, low voltage power supply solutions to drive everything from disc drives to microprocessors. For many of these applications, particularly those that have size constraints, the LT3501® dual step-down converter is an attractive solution because it's compact and inexpensive compared to a 2-chip solution. The dual converter accommodates a 3V to 25V input voltage range and is capable of supplying up to 3A per channel. The circuit in Figure 1 produces 3.3V and 1.8V.

LT3501 Dual Converter Features

- The LT3501 is feature-rich and comes with internal 3.5A switches and sense resistors to minimize solution size and cost.
- The LT3501 operates at a fixed frequency between 250kHz and 1.5MHz, programmed using a single resistor or synchronized to an external clock, allowing optimization of efficiency and solution size.
- A 180° phase relationship between the channels is maintained to reduce input voltage ripple and input capacitor size.
- Independent input voltage, feedback, soft-start and power good functions for each converter simplify the implementation of all the tracking and sequencing options available.
- Minimum input-to-output voltage ratios are extended by allowing the switch to stay on through multiple clock cycles resulting in a 95% maximum duty cycle regardless of switching frequency.
- The LT3501 automatically resets the soft-start function if the output drops out of regulation so that a short circuit or brownout event is graceful and controlled.
- One or both converters can be shutdown at any time if they're not being used, reducing input power drain.
- The LT3501 is available in a 20-pin TSSOP package with an exposed pad for low thermal resistance.



*FOR 3A CAPABILITY ABOVE 16V, INCREASE INDUCTOR VALUE BY 33%.

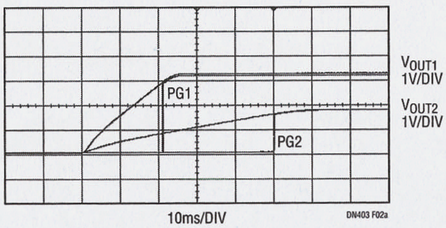
Figure 1. Compact Dual 3A Step-Down Converter with Ceramic Capacitors

Output Supply Tracking and Sequencing

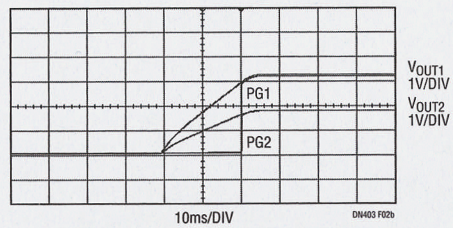
Output voltage tracking and sequencing between channels can be implemented using the LT3501's soft-start and power good pins as shown in Figures 2(a) to 2(c). Output sequencing can also be implemented as shown in Figure 2(d).

High Current Single V_{OUT}, Low Ripple 6A Output

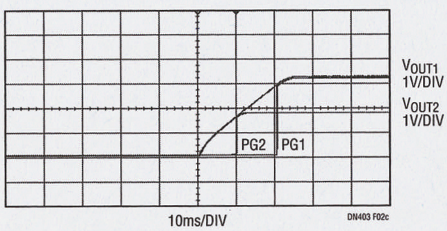
The LT3501 can generate a single, low ripple 6A output as shown in Figure 3 with the dual converters sharing a single output capacitor. With this solution, ripple currents at the input and output are reduced, thus reducing voltage ripple and allowing the use of smaller, less expensive capacitors.



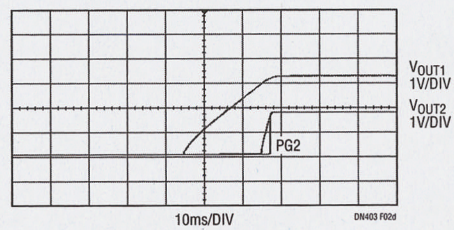
(2a) Independent



(2b) Ratiometric



(2c) Absolute



(2d) Output Sequencing

Figure 2. Output Voltage Tracking and Sequencing

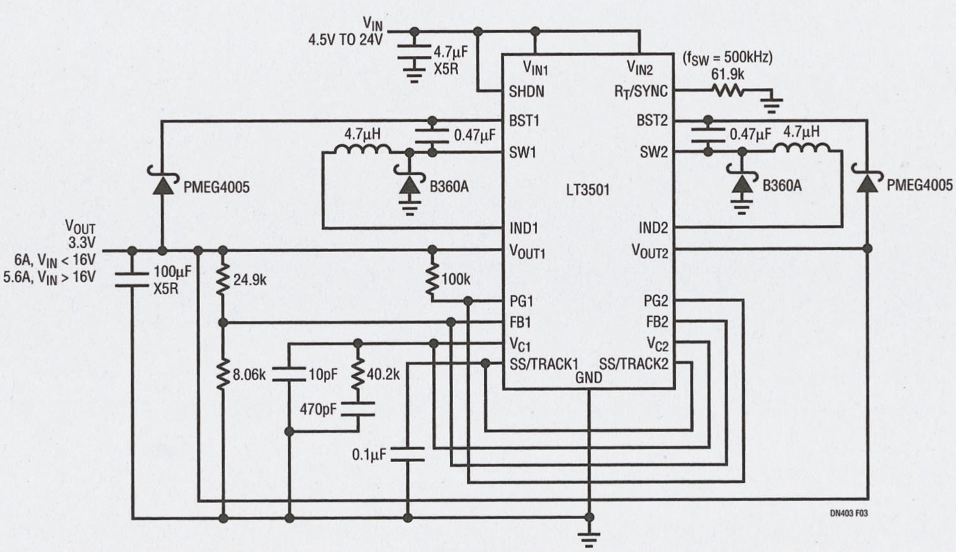


Figure 3. 4.5V to $24V_{IN}$, $3.3V_{OUT}$/6A Step-Down Converter

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LINEAR TECHNOLOGY

Chopper-stabilized amplifier cascade yields 160 to 10,240 programmable gain

Jerome E Johnston, Cirrus Logic Corp, Austin, TX

Certain medical and scientific instrumentation applications require amplification and measurement of microvolt-level signals. For example, accurately measuring the output of a thermopile-based microcalorimeter demands an amplifier that achieves high gain and exhibits excellent thermal stability and low noise.

Figure 1 illustrates how combining two amplifiers yields a programmable-gain amplifier that provides selectable gains of 160 to 10,240. The circuit also offers typical offset voltage of 5 μV, offset drift of 20 nV/°C, and equivalent input-noise voltage of 9 nV$\sqrt{\text{Hz}}$ at 0.1 Hz. IC_1, a Cirrus Logic (www.cirrus.com) CS3301 low-voltage, differential-input, differential-output, chopper-stabilized programmable-gain amplifier, serves as an input-amplifier stage and drives IC_2, a higher voltage INA114 instrumentation-amplifier output stage. The CS3301 provides seven programmable gains of one to 64, and the INA114 provides a fixed gain of 160.

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The combination achieves gains of 160 to 10,240. A thermopile produces a 1-mV signal, yielding 10.24V output from the INA114. To select other values of

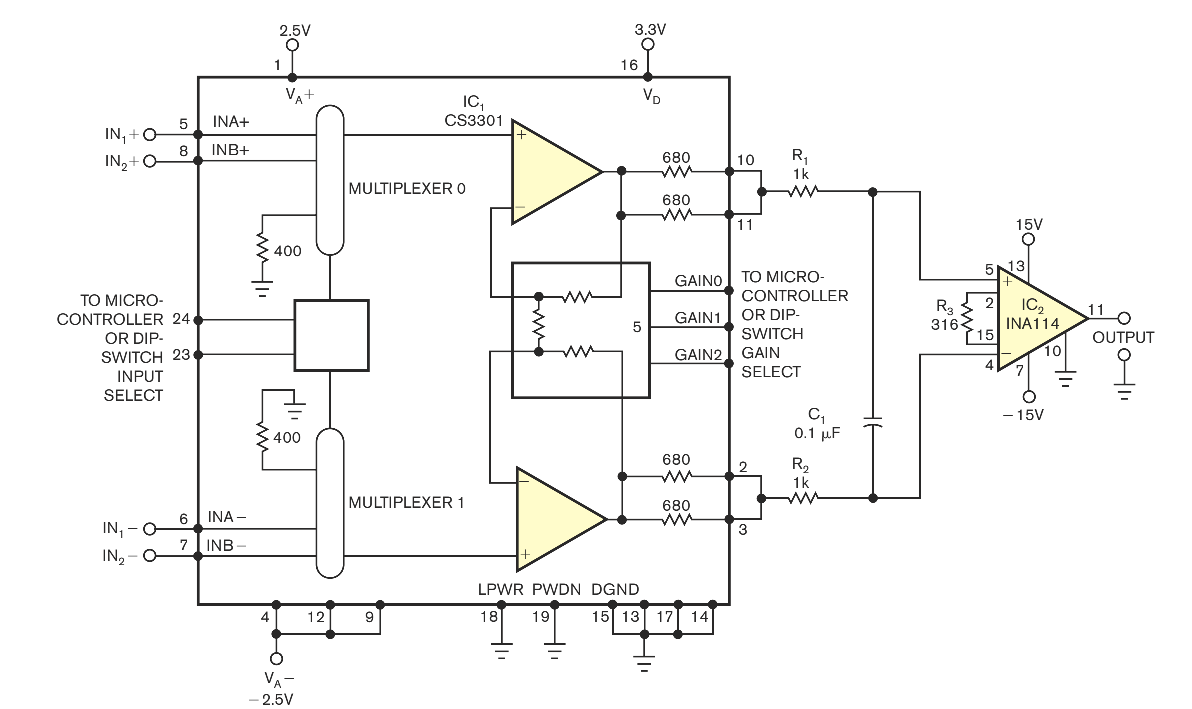

Figure 1 Combining a programmable-gain, chopper-stabilized amplifier with an instrumentation amplifier delivers high gain and low noise over a subaudible frequency range.

gain, change the value of the INA114's gain-setting resistor, R_3.

External DIP switches and pull-up resistors, which connect to the 3.3V supply (not shown), program the CS3301's gain- and multiplexer-control pins. A microcontroller that can drive 3.3V logic can also control these control inputs. Connecting the CS3301's outputs and the INA114's inputs, an RC lowpass filter composed of R_1, R_2, IC_1's output resistors, and C_1 limits noise above 500 Hz.

Figure 2 illustrates the combined amplifiers' measured input-referred noise performance at a gain of 10,000. With its 1/f noise corner at 0.08 Hz, the amplifier cascade achieves an equivalent input-noise voltage of about 9 $nV\sqrt{Hz}$ at 0.1 Hz. The noise-versus-frequency plot represents the results of FFT processing of more than 2 million output samples over an 18-hour period. For simplicity, the schematic doesn't show power supplies and bypass capacitors. Due to the circuit's extreme amplification factor, use construction techniques that maintain thermally balanced component placement and electrically balanced pc-trace lengths.EDN

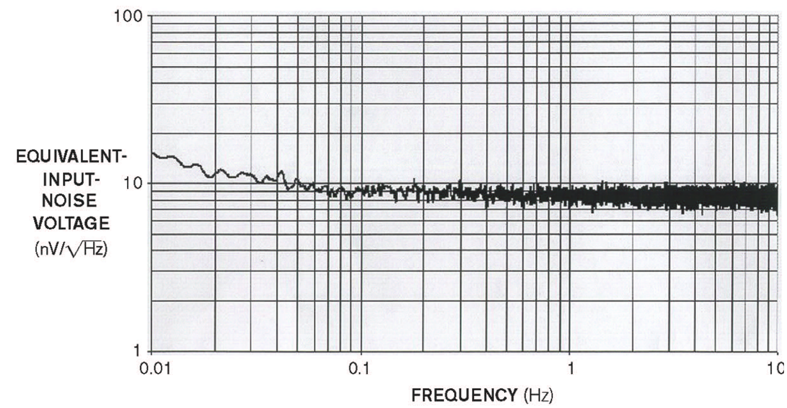

Figure 2 A three-octave plot displays the cascaded amplifiers' low equivalent-input-noise voltage versus frequency.

Current-mode instrumentation amplifier enhances piezoelectric accelerometer

Dave Wuchinich, Modal Mechanics, Yonkers, NY

A typical piezoelectric sensor comprises a disk of PZT-5A ceramic material with metallized electrodes on its surfaces. Applying electrically conductive epoxy to the electrodes connects external wiring to the sensor. An insulating adhesive attaches the assembly to the structure under test and isolates the sensor from ground-referenced potentials. The disk faces the direction of the expected acceleration. When you mount the piezoelectric disk on a target structure, it serves as a simple force sensor and accelerometer by producing a voltage that's directly proportional to the force acting parallel to the disk's direction of polarization. A piezoelectric disk's capacitive impedance presents a large reactance at

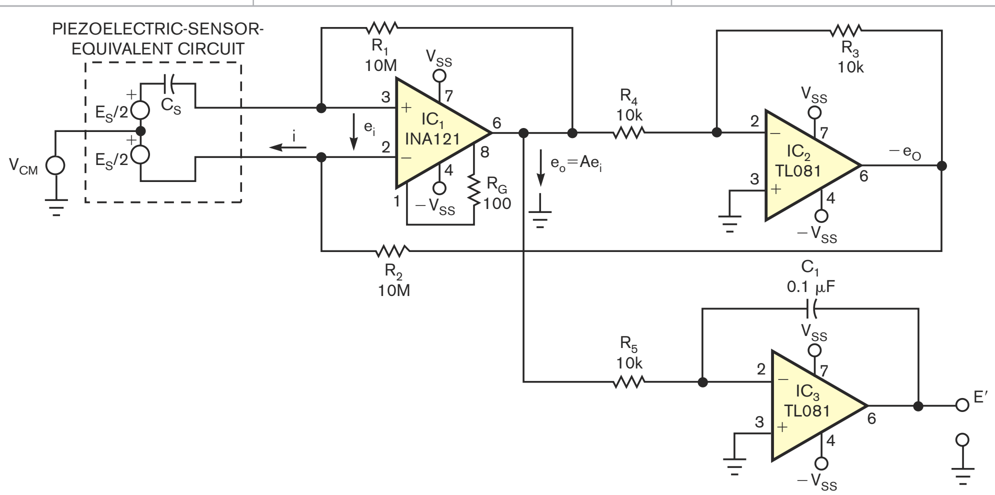

Figure 1 Three amplifiers and a handful of passive components suppress stray noise pickup on a piezoelectric accelerometer and its wiring.

low frequencies, making the disk and its wiring susceptible to interference that surrounding electrical equipment and power lines produce. Placing the sensor in a remote location requires shielded interconnecting cable, but even shielding is not entirely effective in removing common-mode signals because noise pickup can still occur at the disk's conductive surfaces.

One method of extracting the sensor's signal employs an instrumentation amplifier, which amplifies only the potential the sensor produces; the amplifier rejects common-mode-coupled noise potential that appears on each of the sensor's terminals.

A typical miniature piezoelectric-disk sensor that's 0.125 in. in diameter and 0.0075 in. thick presents a capacitance of approximately 500 pF. If the measurement application requires a dynamic response to force excitation frequencies of 10 Hz or below, the sensor's output reactance ranges into the tens of megohms. The circuit's pc-board insulating substrate and ambient humidity impose a practical limit of approximately 10 MΩ on the amplifier's input resistance.

You must carefully choose insulation and apply guarding potentials, and you must use an amplifier with picoampere input-bias currents. Otherwise, the sensor's capacitance and the amplifier's input-bias-current resistors impose a phase shift on the signal you apply to the instrumentation amplifier. To eliminate guarding and elaborate insulation requirements, the circuit in **Figure 1** uses an instrumentation amplifier with feedback to measure the sensor's short-circuit current and not its open-circuit voltage. V_{CM}, the common-mode voltage between the sensor and the signal ground, results from nearby noise sources resulting from stray capacitive coupling. The following **equation** relates the sensor's output current, i, and its open-circuit output voltage, E_S:

$$i=\left[\frac{2A+1}{\left(2R+\dfrac{(2A+1)}{j\omega C_S}\right)}\right]E_S,$$

where A represents IC_1's voltage gain, and $R=R_1=R_2$ in **Figure 1**. Resistors R_1 and R_2 provide feedback and input-bias-current-return paths for IC_1, an INA121 instrumentation amplifier, and resistor R_G sets the amplifier's gain. The INA121's input-bias-offset current of 0.5 pA produces 5 μV of voltage offset across its 10-MΩ feedback resistors. At an amplifier gain of 500, IC_1's output offset amounts to 2.5 mV. Amplifier IC_2, a TL081, provides unity-gain signal inversion.

If $2A+1>>2Rj\omega C_S$, then $i\cong j\omega C_S E_S$, and amplifier IC_1's input voltage, V_1, vanishes because the amplifier's input terminals act as a virtual short circuit across the sensor. Taking the sum of voltages around the loop comprising the instrumentation and inverting amplifiers' output, the two feedback resistors and the instrumentation amplifier's input terminals, whose potential difference is zero, yields $e_O=j\omega R_C E_S$, where e_O represents IC_1's output and also the negative value of IC_2's output.

An operational-amplifier-based integrator, IC_3, delivers the value for E_S at IC_3's output, E′ in the following **equation**.

$$E'=-\frac{RC_S E_S}{C(R_5)}.$$

For the component values in **Figure 1**, IC_1 provides a gain of 500. Resistors R_1 and R_2 are equal at 10 MΩ, and the piezoelectric sensor's capacitance measures 500 pF. For the highest frequency of interest, 10 Hz, the quantity $2R\omega C_S=0.6<<2A+1=501$ and the sensor's output, E_S, appear without phase error as E′. This circuit can measure quasistatic force changes; the circuit's ability to sustain a charge on C_1 imposes the ultimate limit on the circuit's frequency response. EDN

Low-cost RF sniffer finds 2.4-GHz sources

Vladimir Dvorkin, Linear Technology Corp, Milpitas, CA

Whether you measure or use RF circuits that operate in the popular 2.4-GHz ISM (industrial/scientific/medical) band, cordless telephones, Wi-Fi access points, Bluetooth devices, and microwave ovens can radiate RF signals, causing unwanted interference. A spectrum analyzer remains the instrument of choice for detecting and identifying interference sources, but analyzers are expensive, bulky, and sometimes not readily available.

The circuit in **Figure 1** shows an easily assembled, low-cost, and portable RF "sniffer" that provides a quick and reliable reading of the ambient-RF-signal level in the 2.4- to 2.5-GHz frequency band. At the circuit's heart, a Linear Technology (www.linear.com) general-purpose LT5534 RF-power detector, IC_1, measures RF-signal strengths from −55 to −5 dBm and provides an RSSI (received-signal-strength-indicator) dc-output voltage (**Reference 1**).

An antenna for this frequency band drives FL_1, a Toko (www.toko.com) filter (Part No. TDFU2A-2450T-10A), which restricts the circuit's passband to 2.4 to 2.5 GHz and limits out-of-band interference. The filter drives IC_1, whose internal circuitry comprises a cascade of RF detectors and limiters. The detectors' and limiters' summed outputs generate an accurate logarithmic-linear voltage proportional to the RF input in decibels. A single discrete transistor, Q_1, converts IC_1's RSSI output to a current that drives a low-current-LED signal-strength indicator. You can connect a digital voltmeter to IC_1's RSSI output to provide a digital readout of signal strength or rely on the lighted LED to visually indicate an RF signal. Two 1.5V alkaline batteries or three nickel-cadmium cells provide 3V power for the circuit.

The LT5534's frequency range of 50 MHz to 3 GHz covers the VHF, UHF, 800-MHz-cellular-telephone,

902- to 928-MHz-ISM, 2-GHz-PCS (personal-communications-system)/UMTS (Universal Mobile Telecommunications System), and 2.4-GHz-ISM bands. For the 2.4- to 2.5-GHz range, use a Laird Technologies (www.lairdtech.com) BlackChip antenna or a Toko dielectric antenna (Part No. DC2450CT1T). To build a sniffer for the 915-MHz band, replace the antenna with Part No. ANT-916-JJB-ST from Antenna Factor (www.antennafactor.com) and replace the input filter with a Toko 4DFA-915E-10 ceramic filter that provides 26 MHz of bandwidth centered on 915 MHz. EDN

REFERENCE

1 LT5534 data sheet, Linear Technology, www.linear.com.

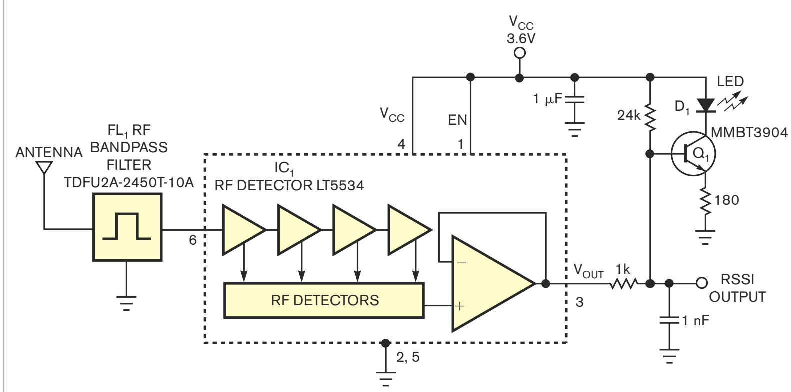

Figure 1 For best results, assemble this 2.5-GHz circuit on a double-sided pc-board layout according to the LT5534's data sheet and application notes.

Triangle waves drive simple frequency doubler

Jim McLucas, Longmont, CO

If you use a function generator, you may occasionally require a sine-wave output at a higher frequency than the generator can provide. If your function generator also produces a triangle-wave output, you can use a frequency doubler to extend the generator's available frequency by as much as a factor of two. A previously published Design Idea describes a triangle-wave-driven frequency-doubler circuit employing op amps that produce output frequencies limited to about 20 kHz (**Reference 1**).

This Design Idea describes a frequency doubler that provides a sine-wave output with a frequency of 4 to 6.7 MHz, with an output level that can range from 110 mV p-p to 1.30 V p-p into a 50Ω load. As **Reference 1** describes, applying a symmetrical triangle wave to a full-wave rectifier produces a triangle wave of twice the input frequency and offset by a dc level. Any asymmetry in the input waveform allows some of the input signal's fundamental frequency to pass through to the output. Also, the circuit's input transformer, T_1, may cause amplitude or phase imbalance, allowing some of the input signal to pass through to the output.

To construct a wideband transformer with good amplitude and phase balance, twist three AWG #30 enameled wires together at about 10 twists/in. Wind seven turns of the bundled wires onto a Fair-Rite (www.fair-rite.com) 2643002402 toroidal core. (Each pass through the core's central opening counts as one turn.) Connect the wires as shown in **Figure 1**. (Refer to **Reference 2** and **Figure 2** for additional information on this type of transformer.) This technique results in a wideband transformer with good amplitude and phase-balance characteristics.

To achieve maximum input-frequency attenuation, use a matched pair of Schottky diodes for D_1 and D_2. However, the prototype produced high-quality signals with unmatched Schottky diodes. In **Figure 1**, diode D_3 applies a small negative bias to D_1 and D_2 that allows operation at low signal levels. Capacitor C_1 passes the rectified and frequency-doubled triangle wave to the bases of a complementary emitter follower comprising Q_3, Q_4, and associated components. A simple, two-element lowpass filter at the follower's output removes higher frequency harmonics. Use any 1.6-µH inductor with a Q of 20 or greater for L_1. Although an inductor with a Q as low as 10 will not noticeably change the filter's frequency response, a value lower than 20 increases the inductor's insertion loss and decreases the maximum available output-signal amplitude.

A simple, two-element, lowpass output filter provides adequate performance for a symmetrical-triangle-wave input because the output's frequency components consist of the doubled input frequency signal and only the desired output signal's odd harmonics. For a 5-MHz output, the third harmonic occurs at 15 MHz with an amplitude of −19 dB relative to the 5-MHz signal. The lowpass filter imposes 15 dB more attenuation at 15 MHz, diminishing the 15-MHz signal to −34 dB relative to the 5-MHz output signal and attenuating higher order harmonics to even lower levels.

The complementary emitter follower's unfiltered output signal consists

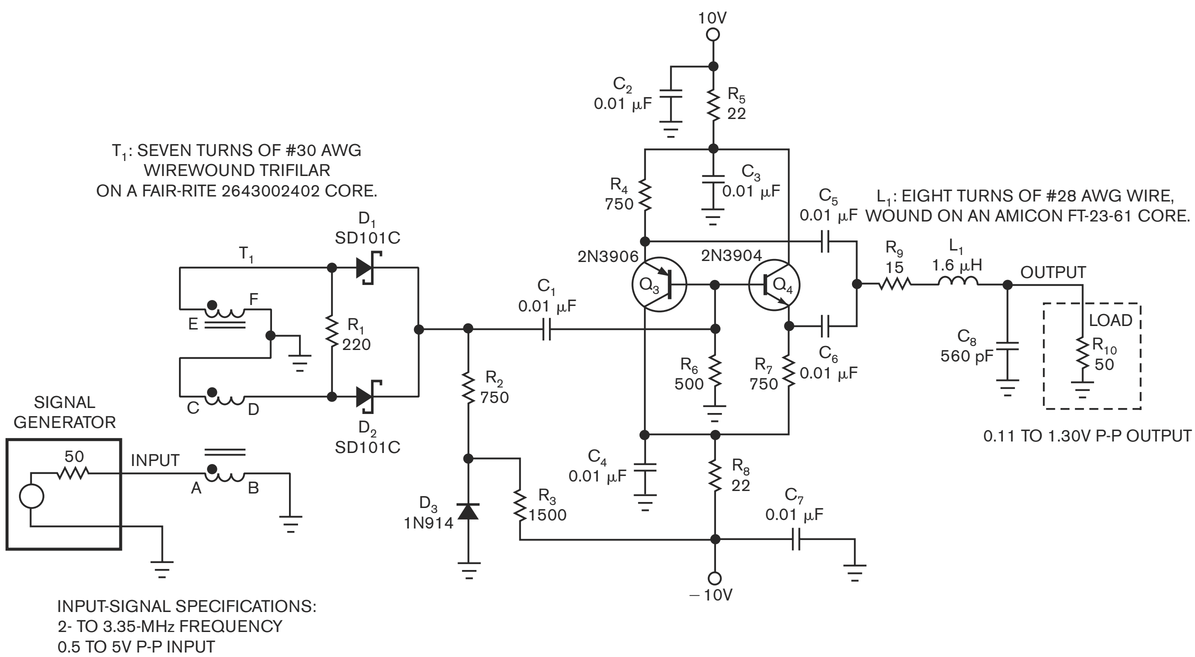

Figure 1 A full-wave rectifier, buffer, and lowpass filter produce a sine-wave output at twice the frequency of a triangular-wave input.

of a triangle wave of twice the input signal's frequency, plus odd harmonics of the doubled input frequency. For example, applying a 2.5-MHz triangle wave to the circuit's input produces a 5-MHz triangle-wave signal at the lowpass filter's input. For a nearly perfect triangle wave, the filter's input consists of a 5-MHz fundamental and only its odd harmonics. At −19 dB below the 5-MHz signal, the 15-MHz third harmonic represents the closest spurious signal and one that you can easily filter.

To use the circuit at higher frequencies, divide the values of output-filter components L_1 and C_8 by a factor of $F_{NEW}/5$, where F_{NEW} represents the desired output frequency in megahertz. For example, a nominal output frequency of 20 MHz requires division of the values of L_1 and C_8 by a factor of four, producing new values of 0.4 μH and 140 pF, respectively. Simulating the circuit with the revised filter in Spice shows adequate harmonic rejection over an output range of 16 to 26.8 MHz. Although designed for 5-MHz operation, the remainder of the circuit works well at 20 MHz without additional modifications. This frequency doubler also accepts a sine-wave input signal. However, the circuit's unfiltered output contains higher levels of the desired signal's even- and odd-order harmonics and requires additional filtering to produce a high-quality sine-wave output. **EDN**

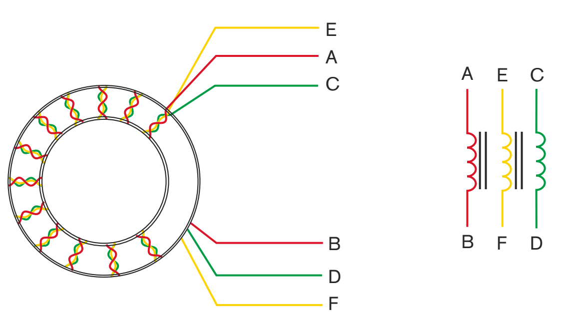

Figure 2 Transformer T_1 from Figure 1 consists of three windings on a toroidal ferrite core. For ease of assembly, twist three wires of different colors into a bundle to form the windings.

REFERENCES

1 Belousov, Alexander, "Frequency doubler operates on triangle waves," *EDN*, March 14, 1996, www.edn.com/archives/1996/031496/06di4.htm.

2 Demaw, MF "Doug," *Applying Toroidal Cores: Ferromagnetic-Core Design and Application Handbook*, ISBN: 0133140881, Prentice Hall, 1996, pg 97.

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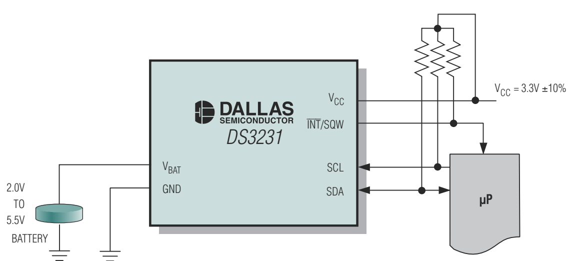

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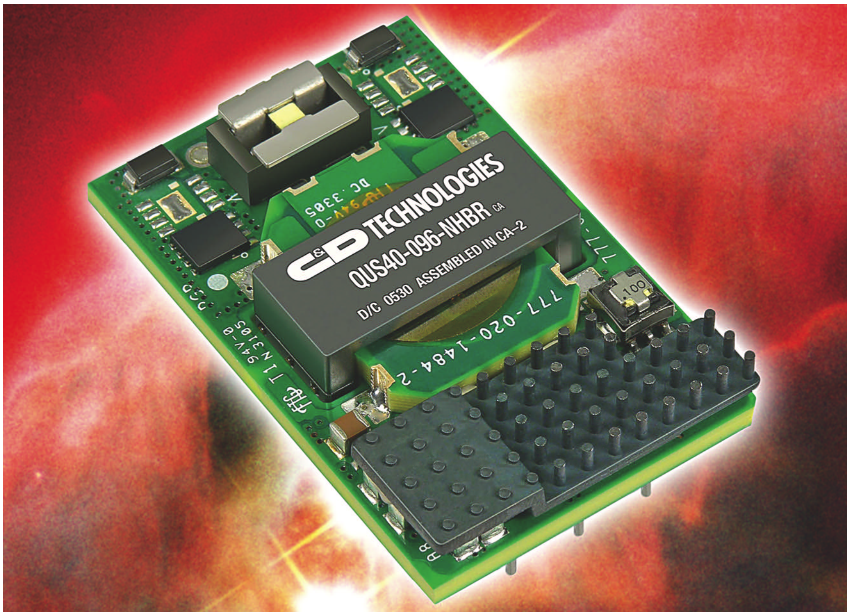

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Providing a 5-to-1 fixed-conversion ratio, the QUS40-096 dc/dc converter delivers 300W maximum output power at a 38V dc input, 55°C, and 200-lfm airflow. Rendering a 96.6% typical efficiency, the converter operates from a 48V-dc typical input voltage and features a 9.6V-dc output-voltage setpoint and 2250V isolation-plus-protection circuitry with auto-restart. Available in a quarter-brick-footprint package, the device targets use in intermediate-bus-architecture applications. The QUS40-096 costs $54.78 (1000).

C&D Technologies, www.cd4power.com

Integrated buck converter targets low-power and portable applications

Aiming at smart phones, personal media players, and mobile-gaming platforms, the EP53x2Q integrated dc/dc-buck-converter family operates at a 5-MHz switching frequency, reducing the size of filter components. The devices combine a PWM controller, MOSFET switches, a compensation network, and a power inductor in a 5×4×1.1-mm QFN package. The converter requires two ceramic filter capacitors. A three-pin voltage-select scheme programs the voltage output, allowing a designer to choose one of seven predefined voltages or to use an external divider. Designers can also change the voltage-select pins to implement dynamic-voltage scaling. Available in 500, 600, and 800-mA load currents, the EP53x2Q converters cost $1.50, $1.55, and $1.61, respectively.

Enpirion, www.enpirion.com

Encapsulated ac/dc power modules come in miniature packages

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POWER SOURCES

ries of 15 and 30W encapsulated ac/dc power-supply modules suits space-critical applications in industrial, medical, and OEM equipment. Packaging and mounting styles include a pc board with solder pins, a chassis mount with screw terminals, and a DIN-rail-mount-adapter kit. The pc-board version measures 2.17×1.77×0.95 in. for the 15W unit and 2.99×2.01×1.1 in. for the 30W unit. The Tracopower TMT series costs $38 (100).

Power Sources Unlimited, www.psui.com

COTS dc/dc converters target defense and avionics applications

The 4 to 30W MTC series of dc/dc converters aim at defense and avionics applications. Based on COTS (commercial-off-the-shelf) components, these converters come in 5, 15, and 35W ratings. Suiting systems with nominal 28V inputs, the converters have a 15.5 to 40V input range and operate through 10V transients for 10 sec and 50V transients for 1 sec, in accordance with military standard 704B-F. The MTC costs $120 (100) for the 4W unit and $260 (100) for the 35W unit.

XP Power, www.xppower.com

SIP converters come in a miniature package

Providing 6-kV-dc I/O isolation, the 1W D100EHI miniature converter series comes in a miniature SIP-7 package. The 16 models operate from 5 and 12V-dc inputs and provide 5, 9, 12, 15, ±5, ±9, ±12, or ±15V dc. Features include an internal filter, 81% efficiency, low-noise operation, and an MTBF greater than 3.5 million hours. The D100EHI family costs $4.10 (100).

MicroPower Direct, www.micropowerdirect.com

COMPUTERS AND PERIPHERALS

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Itronix, www.gobookxr-1.com

Desktop autoloader delivers 560 Gbytes of backup

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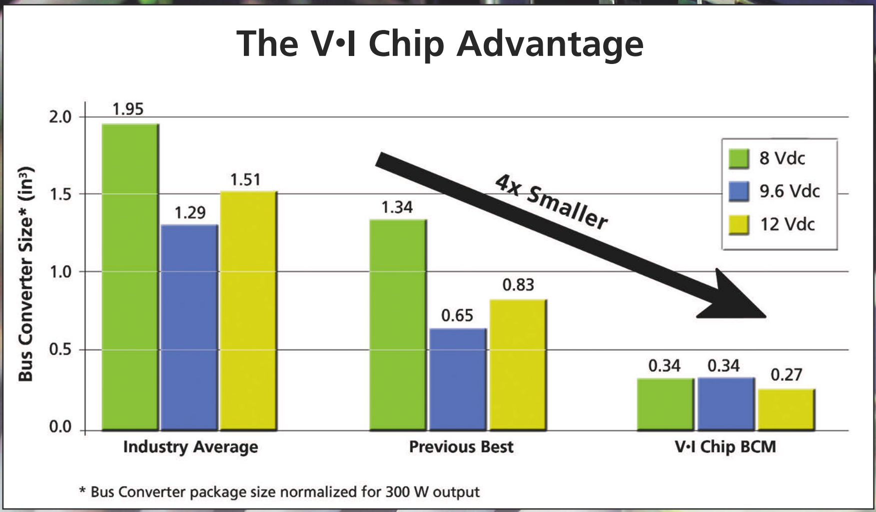

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B048F080T24	8.0	240 W	96.0
B048F096T24	9.6	240 W	96.2
B048F120T30	12.0	300 W	95.1
B048F160T24	16.0	240 W	96.0
B048F240T30	24.0	300 W	95.7
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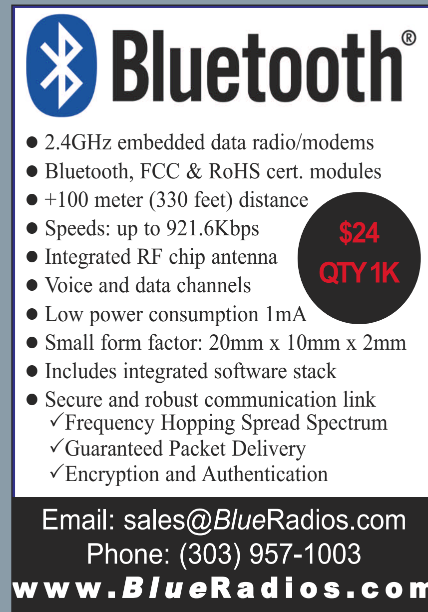

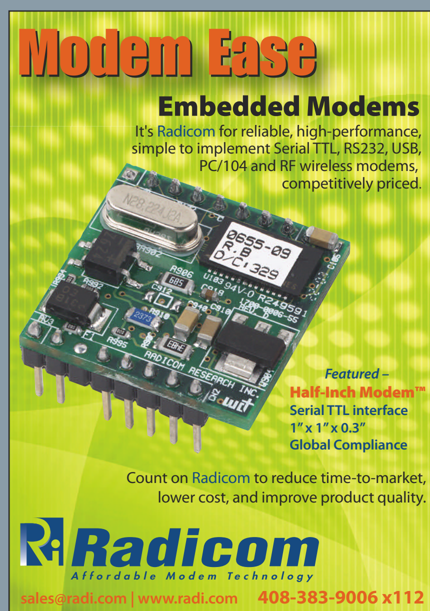

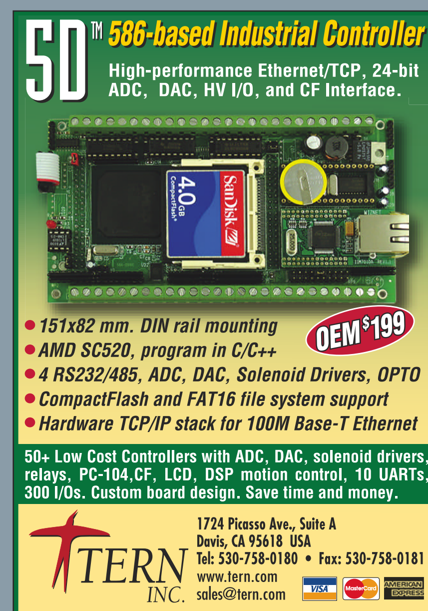

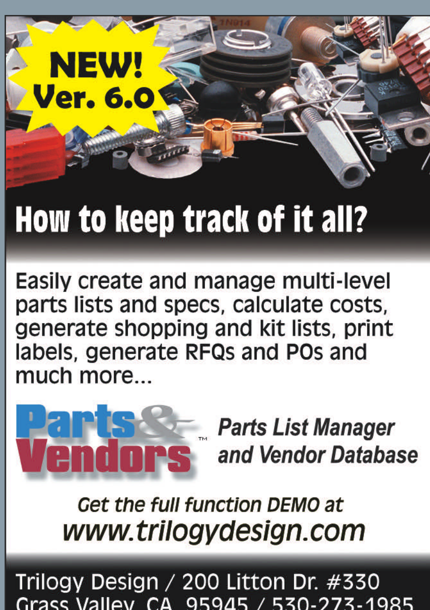

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Iomega, www.iomega.com

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Adaptec, www.adaptec.com

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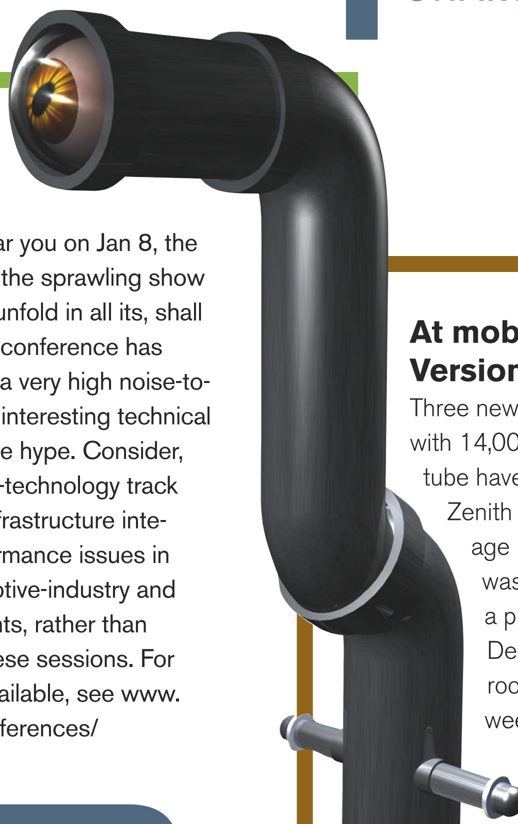

LOOKING AHEAD

To the Consumer Electronics Show

Coming to a Las Vegas near you on Jan 8, the 40th-anniversary edition of the sprawling show of consumer products will unfold in all its, shall we say, assertiveness. The conference has something of a bad rap for a very high noise-to-information ratio, but some interesting technical tracks lie buried beneath the hype. Consider, for instance, an automotive-technology track with sessions on vehicle-infrastructure integration and on driver-performance issues in vehicle electronics. Automotive-industry and academic R&D heavyweights, rather than marketing folks, present these sessions. For a broader look at what's available, see www.cesweb.org/attendees/conferences/knowledge_tracks.asp.

LOOKING BACK

At mobile television, Version 1.0

Three new portable-television receivers with 14,000V applied to the picture tube have been announced by the Zenith Radio Corp. This high voltage is claimed to end the milky, washed-out pictures that are a problem with portable TV. Designed to be used in any room of the house or taken on weekend outings, the sets are carried luggage-style, with the face tube up. One can see that this presents the opportunity for the most avid of TV viewers to keep an eye glued to the picture while in transit, provided, of course, that a long extension cord is available or a small back-pack generating plant is part of one's normal attire.

—*Electrical Design News*, November 1956

LOOKING AROUND

AT MOBILE TELEVISION, VERSION 2006.11.23

If we are to believe our e-mail, approximately 723 companies are rushing to prepare mobile-video-reception and -display silicon. All this activity seems to have bypassed the question of in just which applications mobile-video products might find use. Physics, or at least the urge for self-preservation, would seem to preclude watching soap operas while actually moving around. In reality, wireless-channel characteristics will probably have a similar impact through their limitations on quality of service. So, are we really talking about transportable fixed video viewers, with 5-cm screens and four-hour battery lives?

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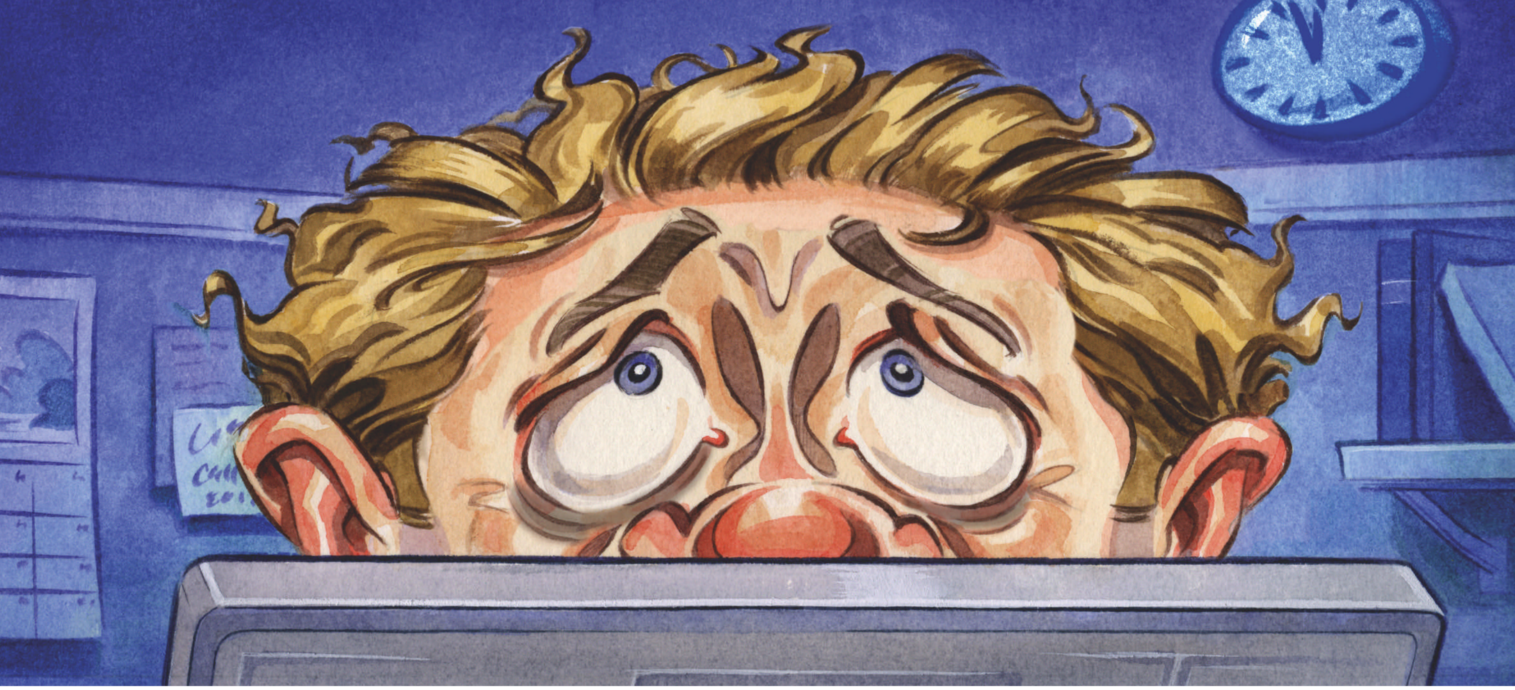

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